

Quincy Flint

Virtual Memory

EEL 3713C: Digital Computer Architecture

Quincy Flint

[Ionospheric Radio Lab in NEB]

Outline

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1. Memory Problems

- Not enough memory
- Holes in address space
- Programs overwriting

2. What is Virtual Memory?

- Layer of indirection
- How does indirection solve above
- Page tables and translation

3. How do we implement VM?

- Create and store page tables
- Fast address translation

4. Virtual Memory and Caches

- Prevent cache performance degradation when using VM

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Multi-Level Page Tables

Page Table Size... again

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- Given a 32-bit machine, 4 kB pages...

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- Given a 32-bit machine, 4 kB pages...
 - 1 million PTEs
 - $32 \text{ bits (machine)} - 12 \text{ bits (page offset)} = 20 \text{ bits} = 1 \text{ million}$

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 $= 4 \text{ MB page tables}$

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Page Table Size... again

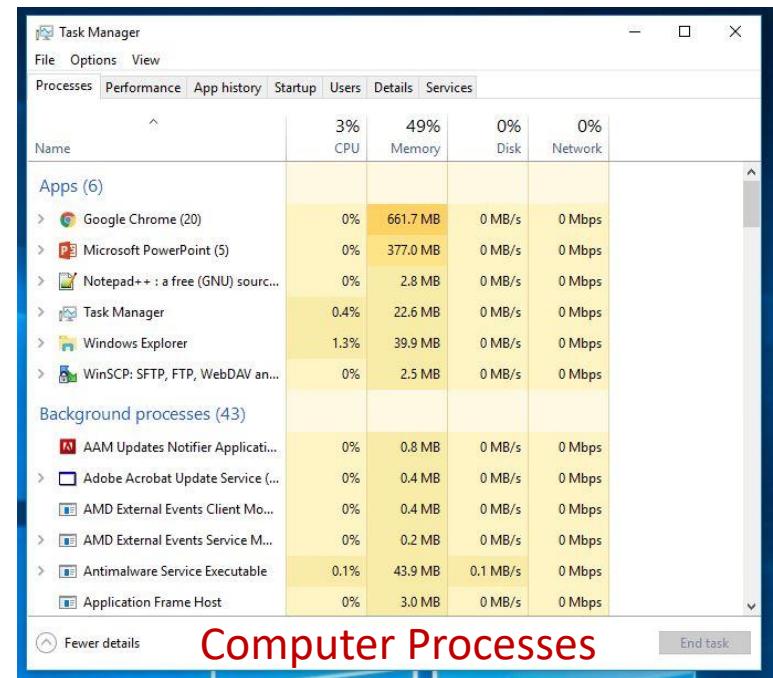
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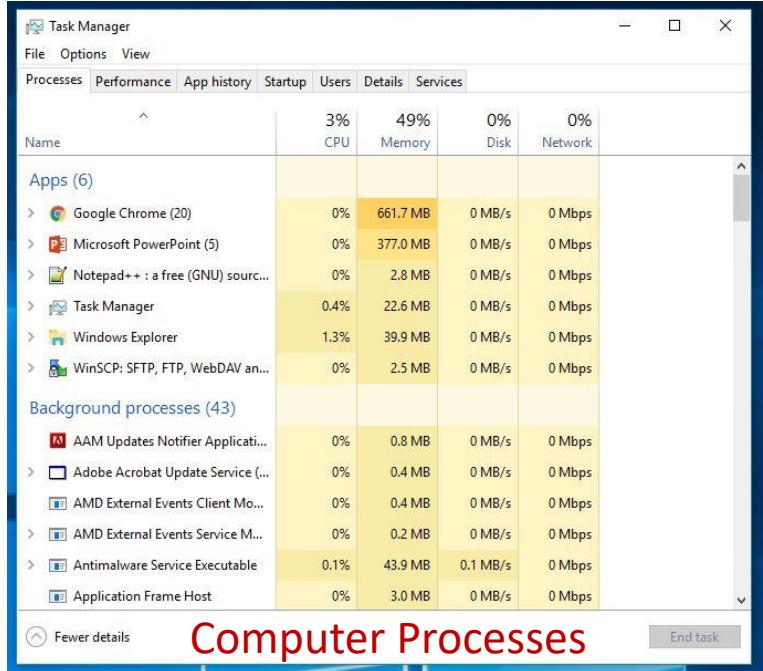
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1M entries x 4 Bytes per entry
= 4 MB page tables

4 MB page tables x 50 processes
= 200 MB of RAM for PTs



A screenshot of the Windows Task Manager showing the "Processes" tab. The table displays various running programs and their resource usage. The columns are labeled: Name, CPU, Memory, Disk, and Network. The "Memory" column shows values such as 661.7 MB, 377.0 MB, etc.

Name	3% CPU	49% Memory	0% Disk	0% Network
Apps (6)				
> Google Chrome (20)	0%	661.7 MB	0 MB/s	0 Mbps
> Microsoft PowerPoint (5)	0%	377.0 MB	0 MB/s	0 Mbps
> Notepad++ : a free (GNU) sour...	0%	2.8 MB	0 MB/s	0 Mbps
> Task Manager	0.4%	22.6 MB	0 MB/s	0 Mbps
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> WinSCP: SFTP, FTP, WebDAV an...	0%	2.5 MB	0 MB/s	0 Mbps
Background processes (43)				
> AAM Updates Notifier Application	0%	0.8 MB	0 MB/s	0 Mbps
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> AMD External Events Client Mo...	0%	0.4 MB	0 MB/s	0 Mbps
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> Antimalware Service Executable	0.1%	43.9 MB	0.1 MB/s	0 Mbps
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Computer Processes

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Computer Processes

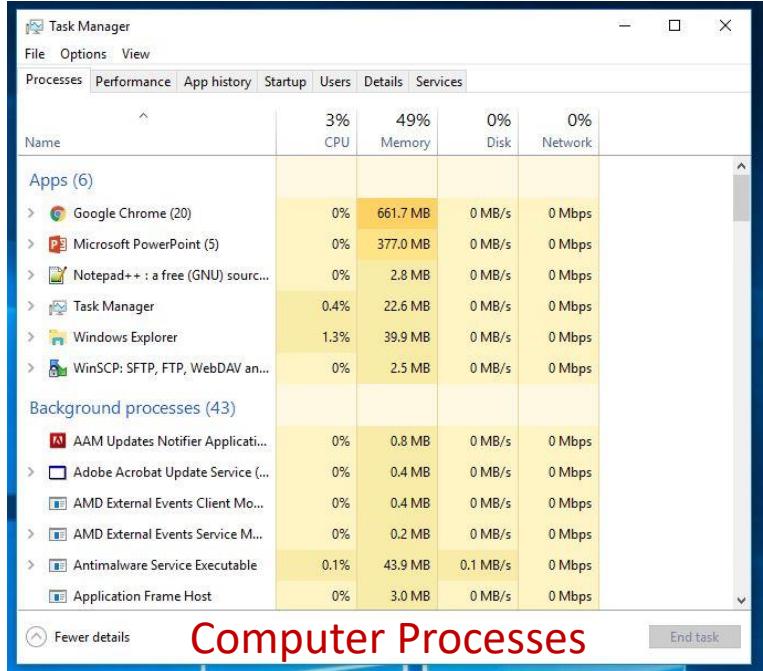
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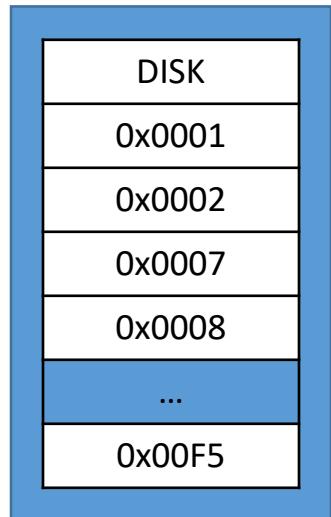
Computer Processes

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Multi-Level Page Tables

1st Level Page Table
4kB [1,024 entries]

Size of 1 Page



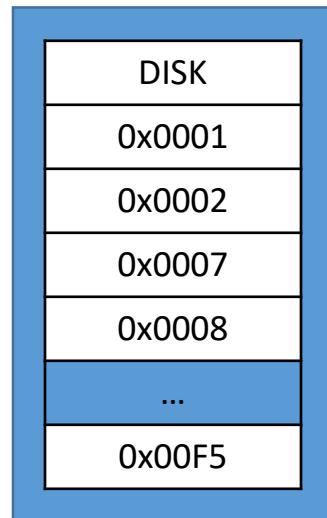
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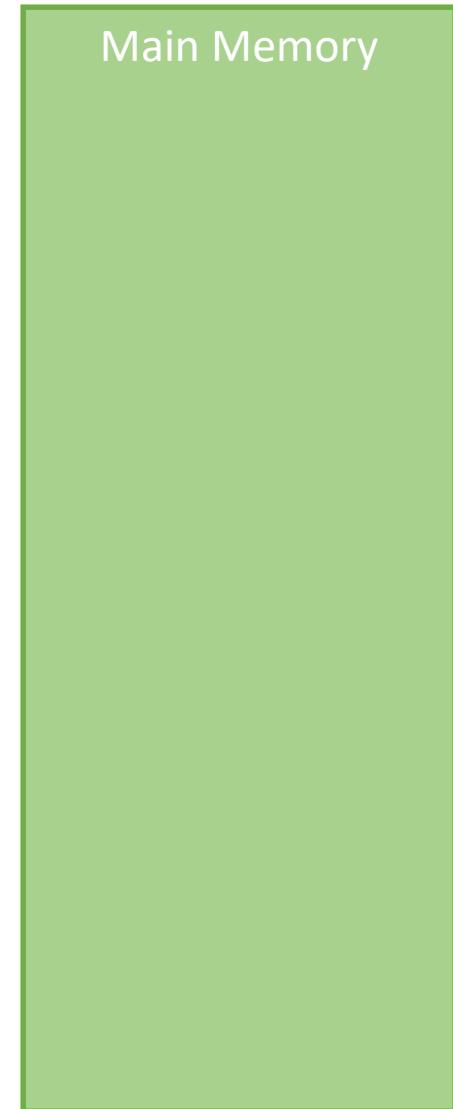
Size of 1 Page



2nd Level Page Table

4kB each [1,024 entries]

Main Memory

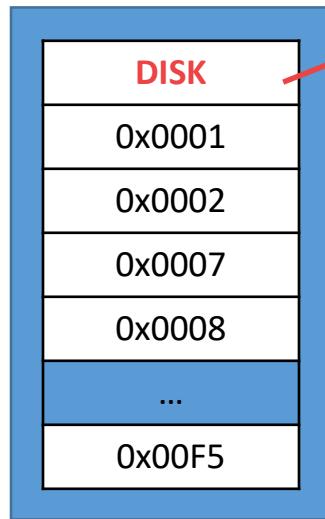


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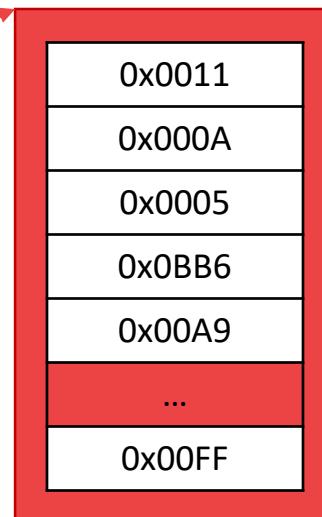
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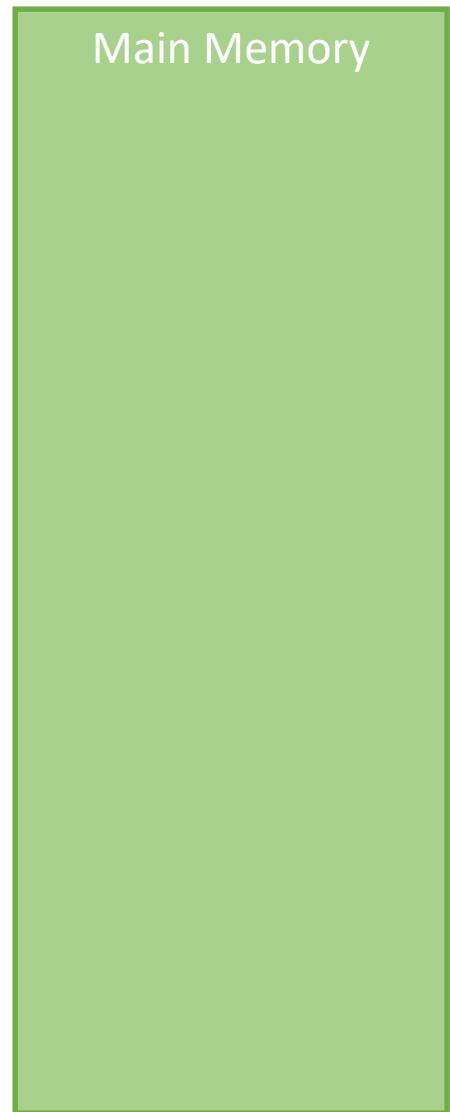
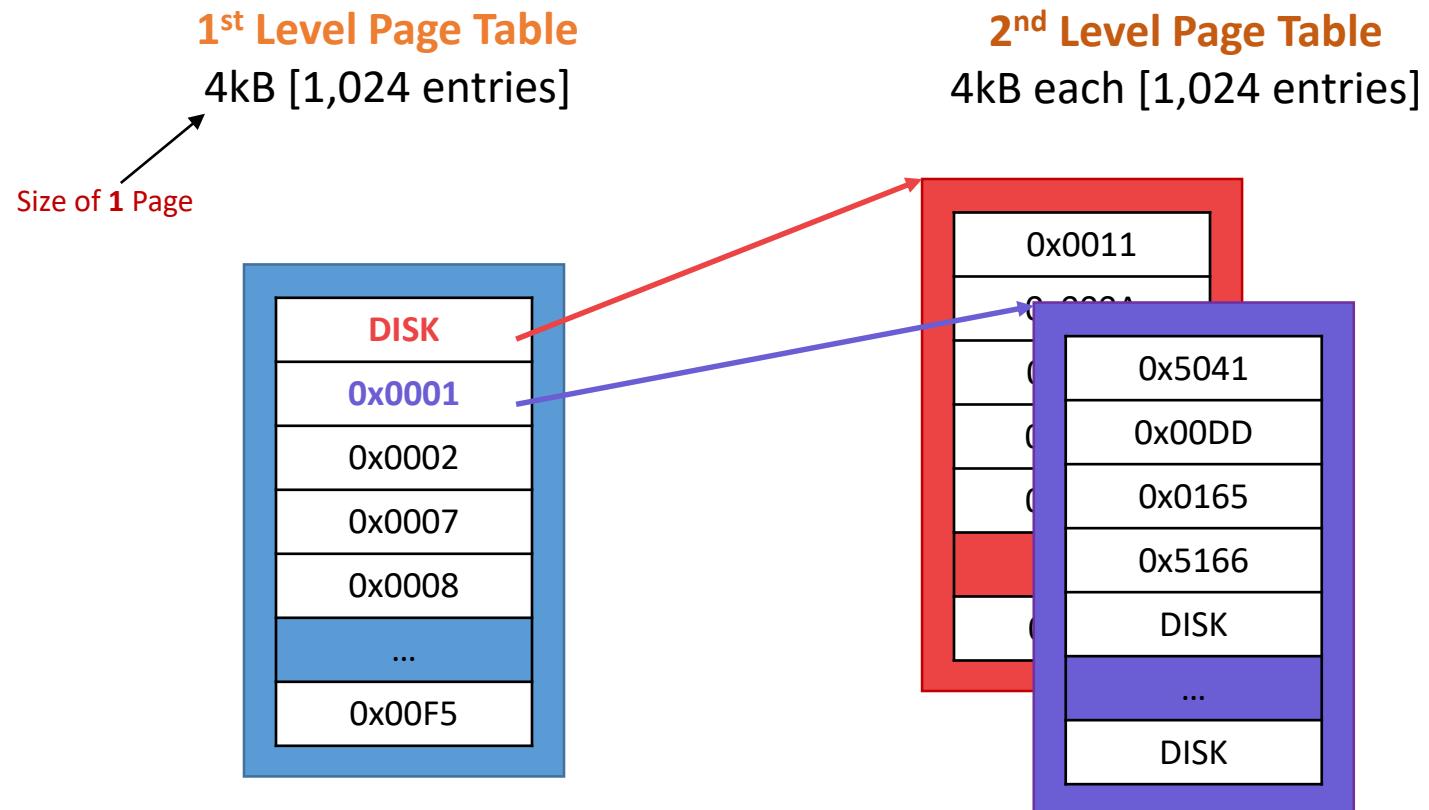


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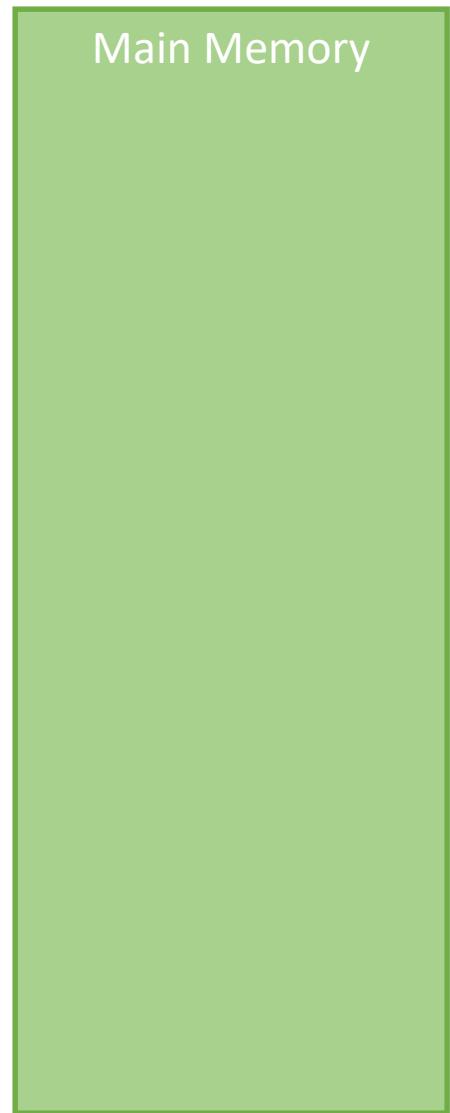
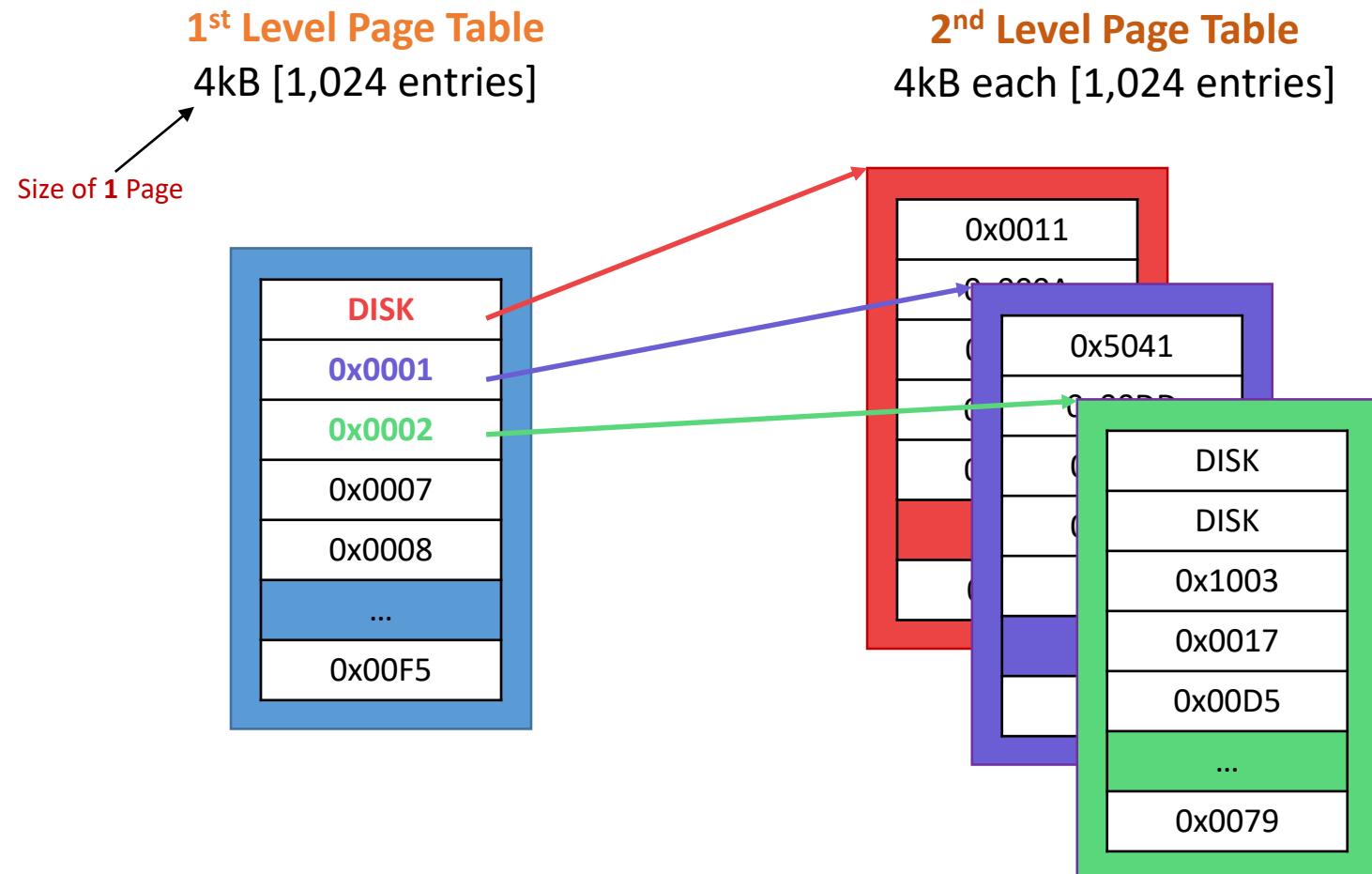
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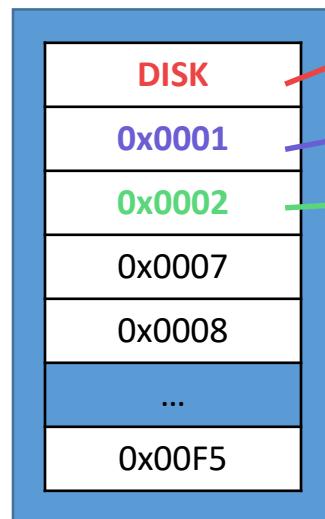


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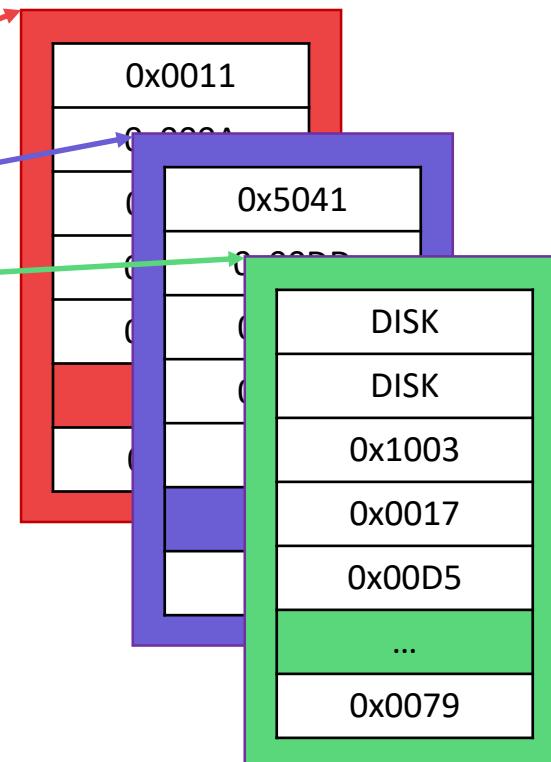
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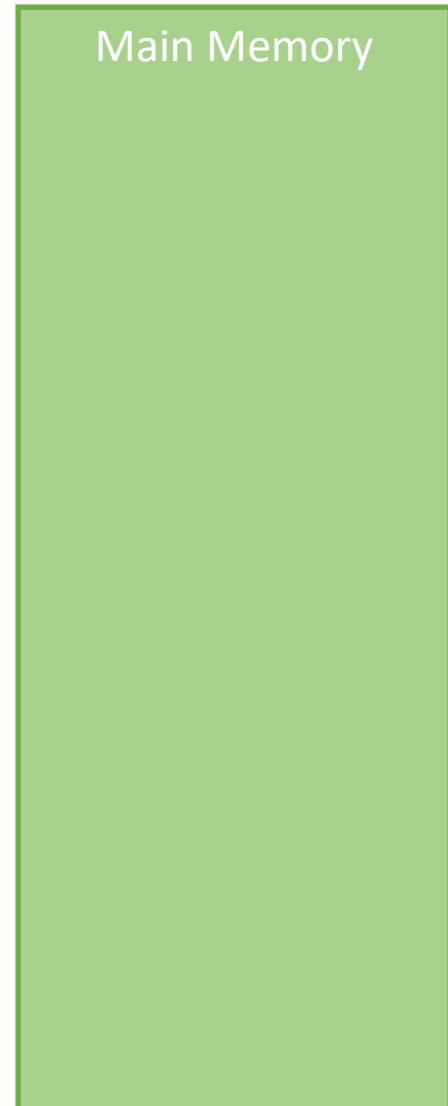


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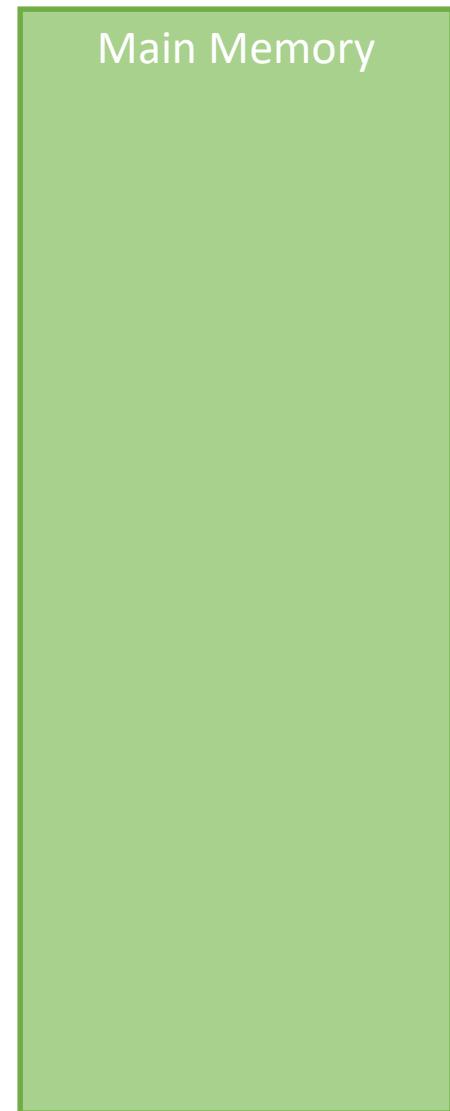
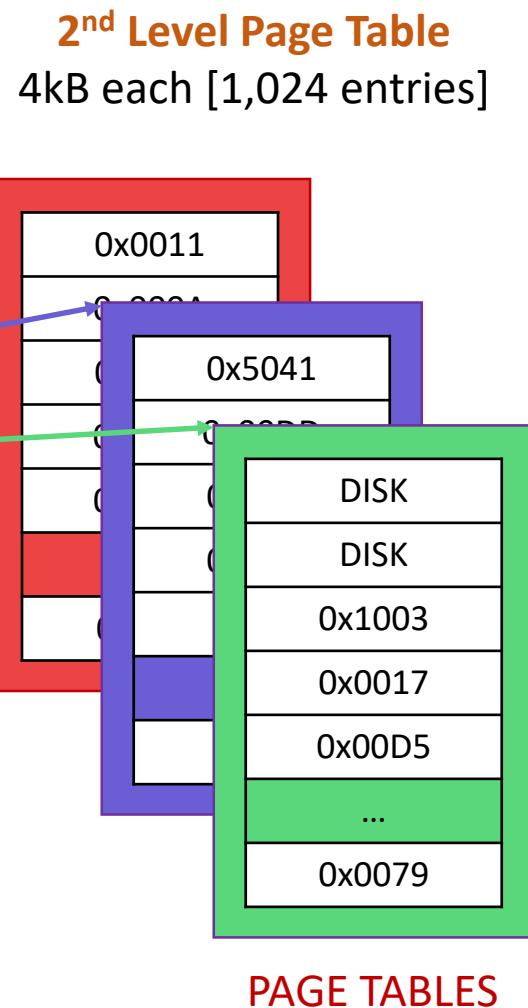
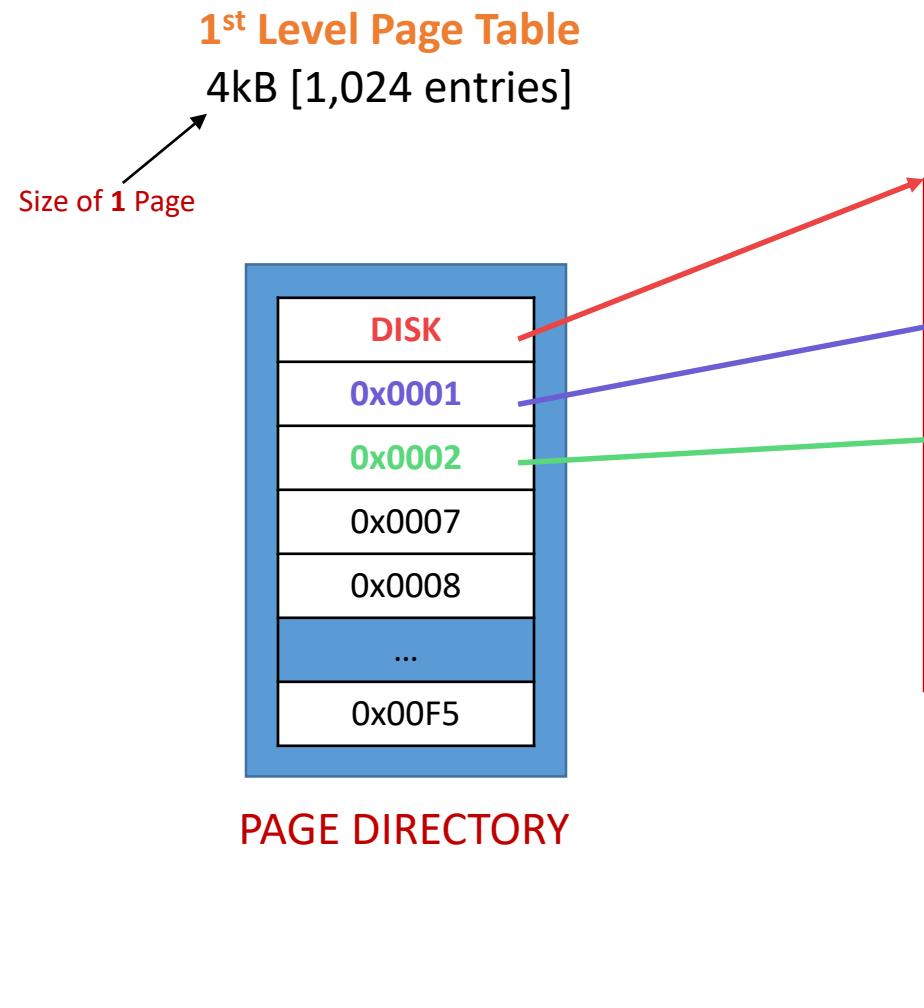
PAGE TABLES

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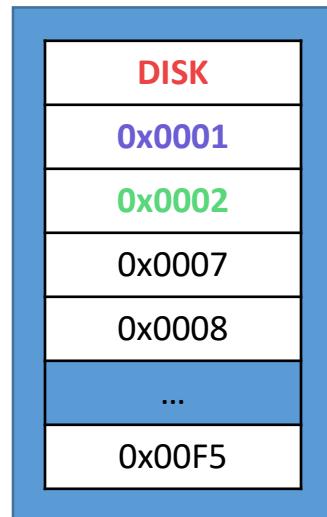


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PAGE DIRECTORY

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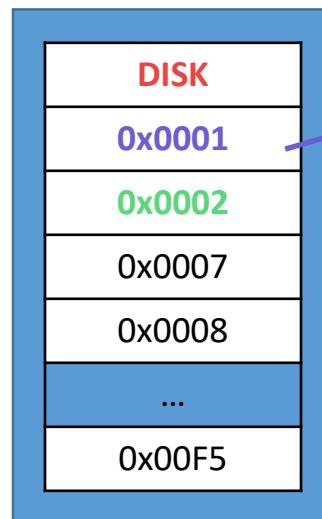
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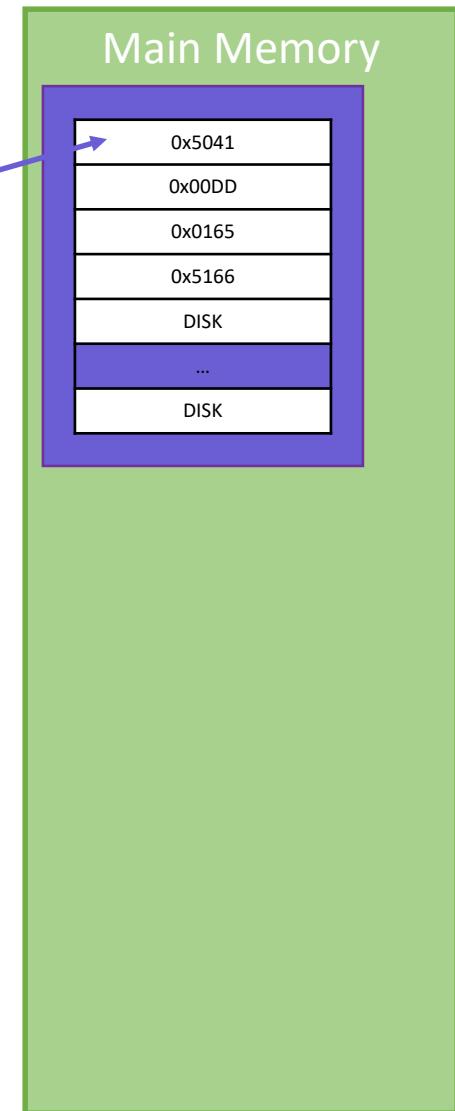
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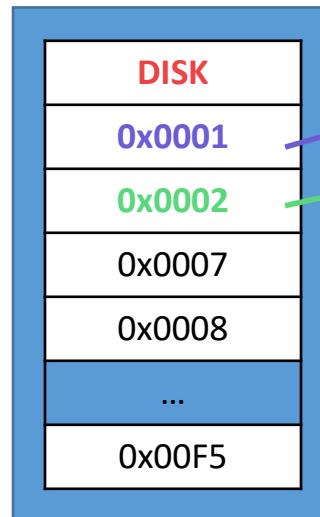


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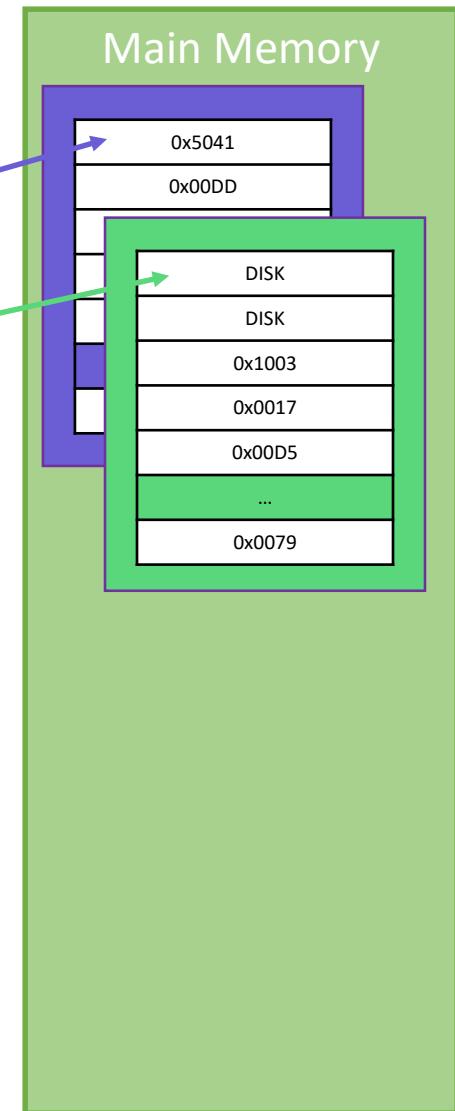
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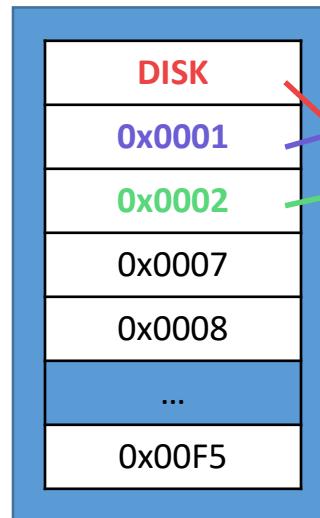


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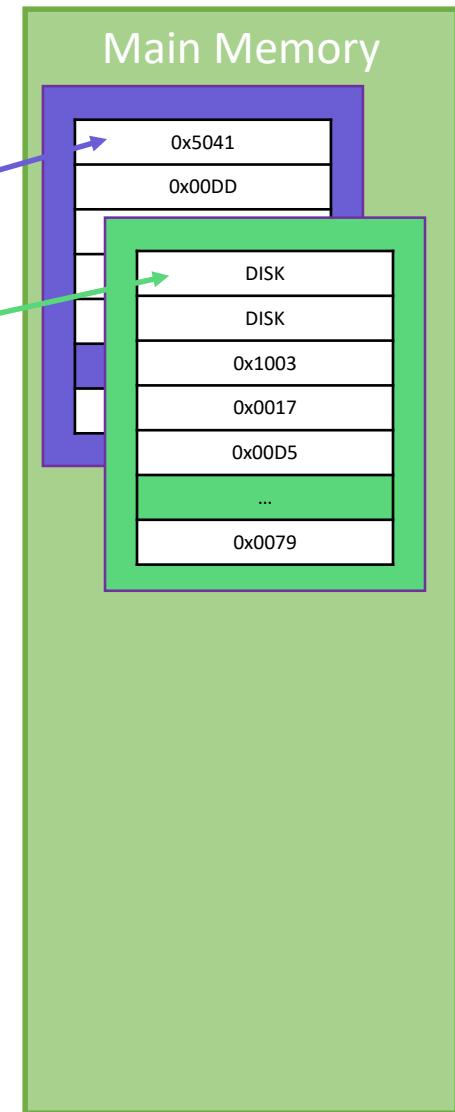
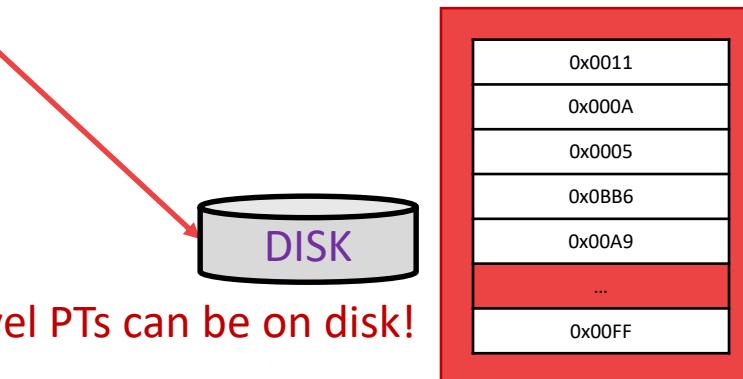
Size of 1 Page



PAGE DIRECTORY

2nd Level Page Table
4kB each [1,024 entries]

2nd level PTs can be on disk!



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Multi-Level Page Tables

1st Level Page Table
4kB [1,024 entries]

Size of 1 Page

DISK
0x0001
0x0002
0x0007
0x0008
...
0x00F5

PAGE DIRECTORY

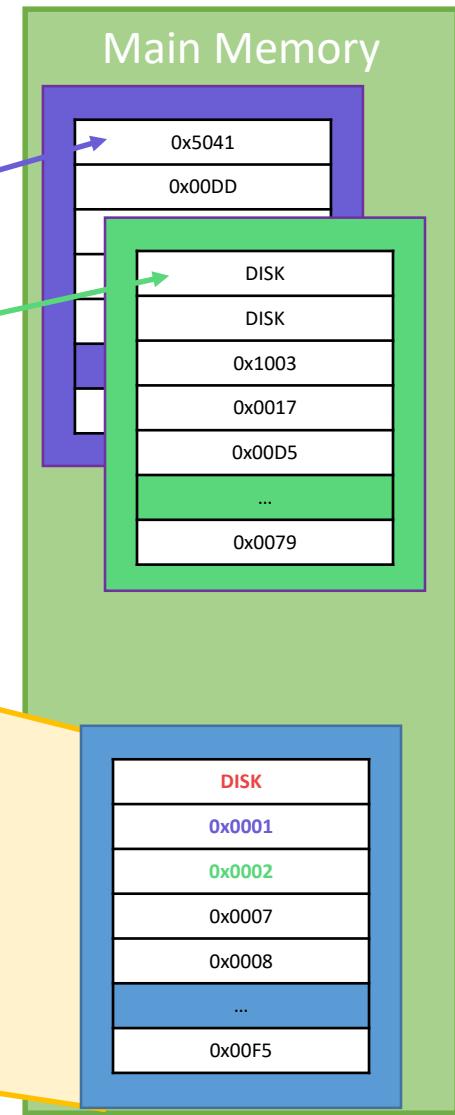
2nd Level Page Table
4kB each [1,024 entries]

As long as 1st level PT is in RAM,
we can find all 2nd level PTs!

2nd level PTs can be on disk!



0x0011
0x000A
0x0005
0x0BB6
0x00A9
...
0x00FF



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Quiz: Multi-Level Page Tables



Q: With multilevel page tables, what is the smallest amount of page table data that we need in RAM to run a single 32-bit application?

- I. 4 kB
- II. 8 kB
- III. 8 MB
- IV. 1 GB
- V. 4 MB

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A:

- II. 8 kB

We must always keep the 1st level page table in RAM (4 kB) and we need at least the 2nd level page table for the application data.

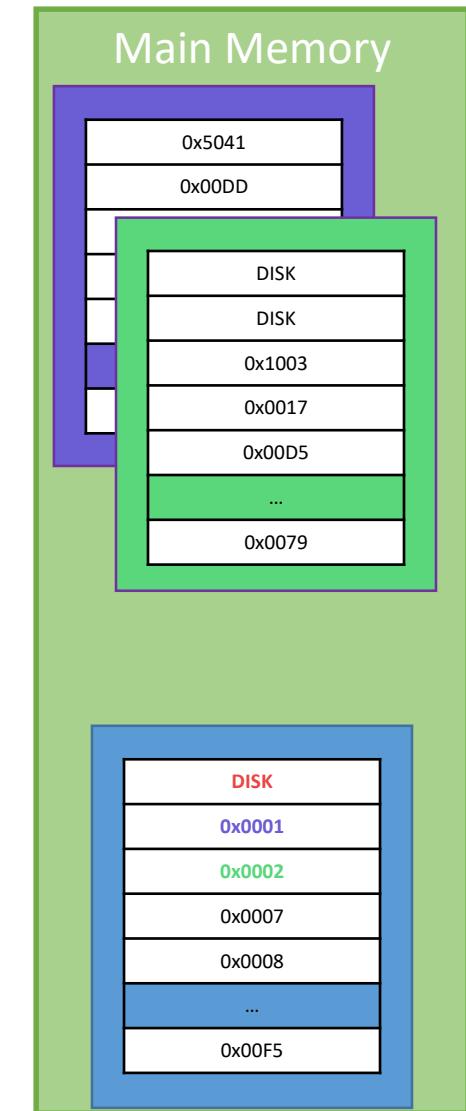
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Multi-Level Page Table Translation

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Physical Address [28 bits]



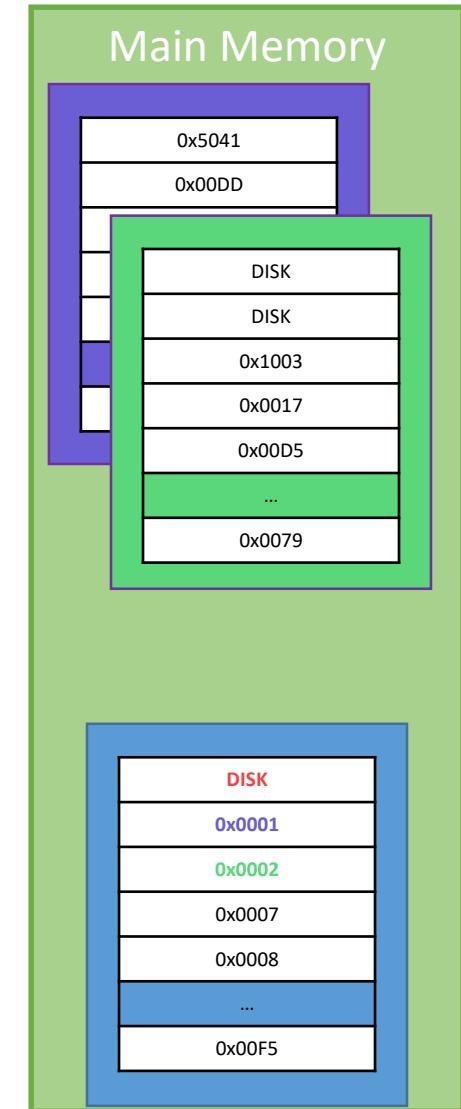
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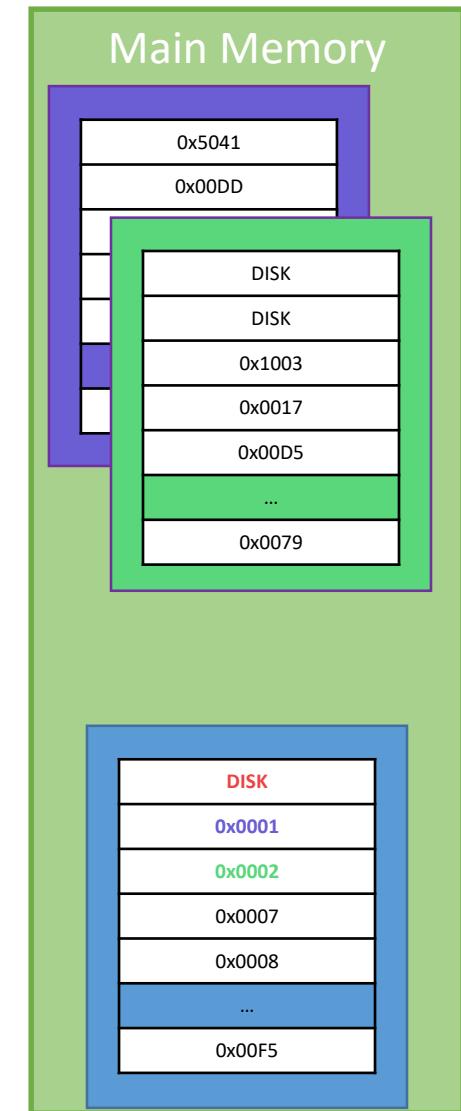
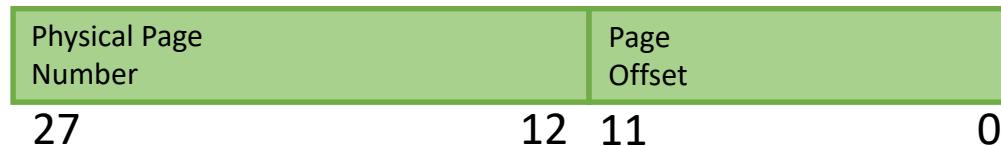
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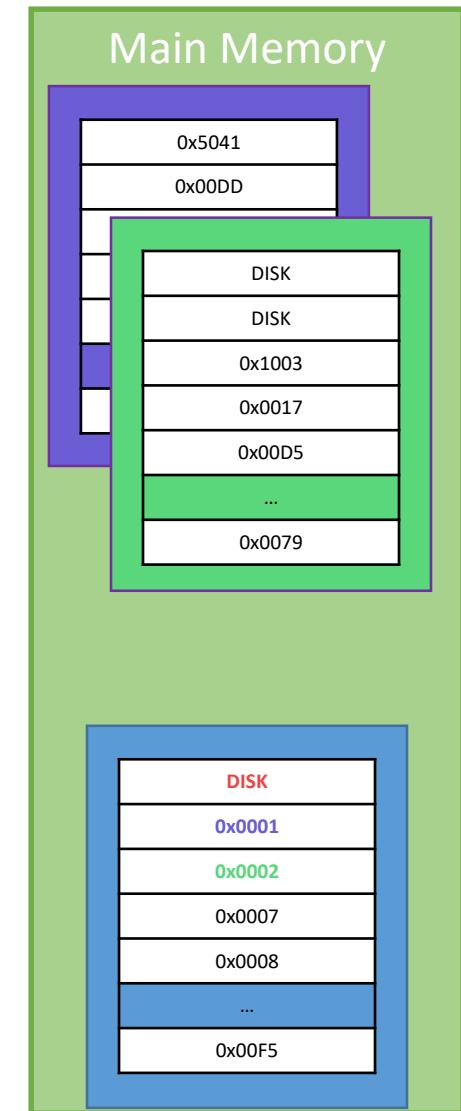
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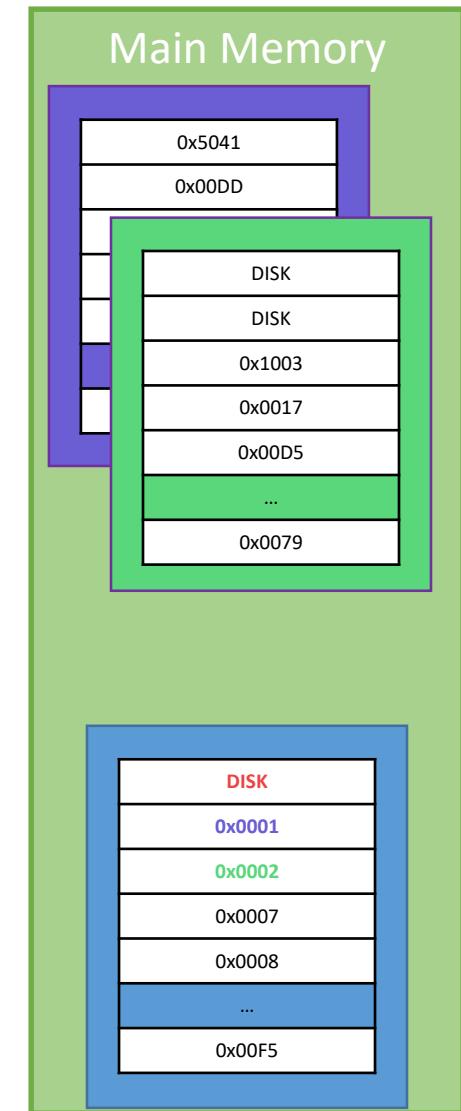
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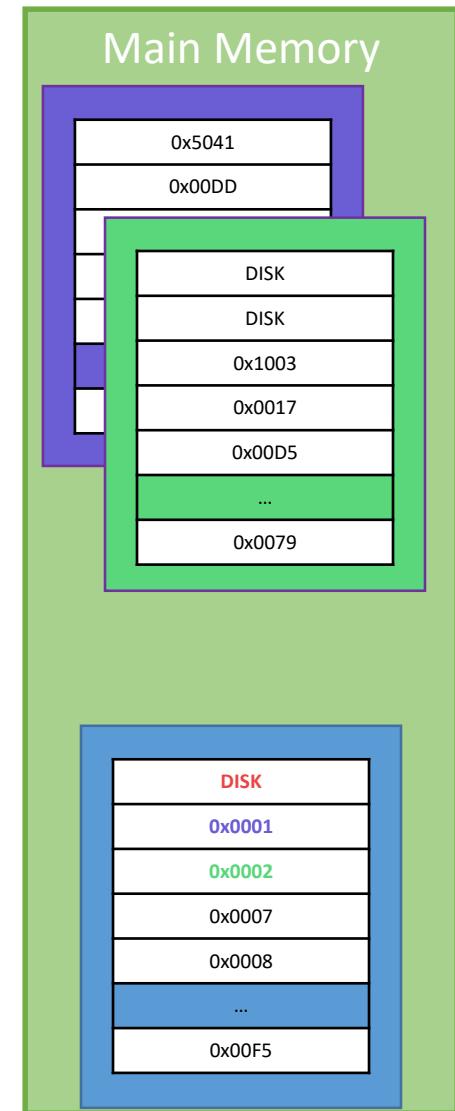
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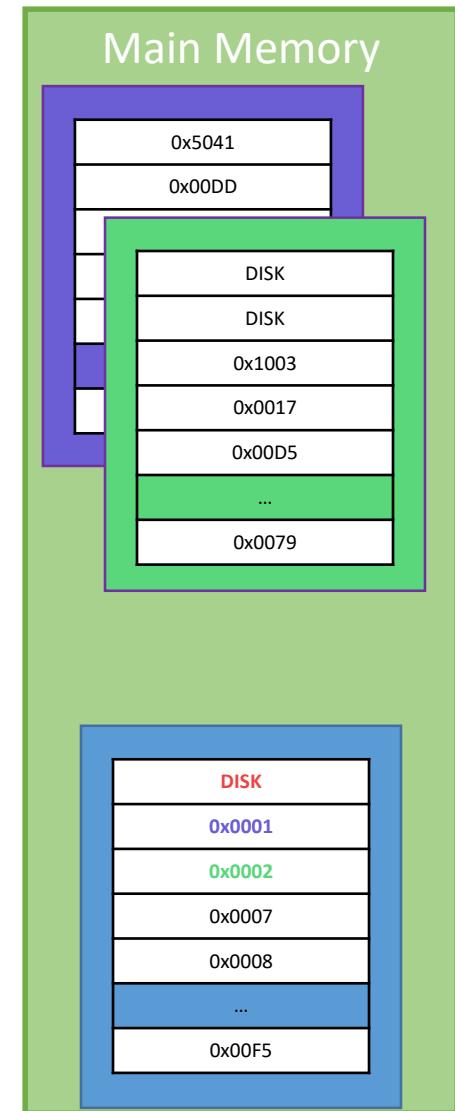
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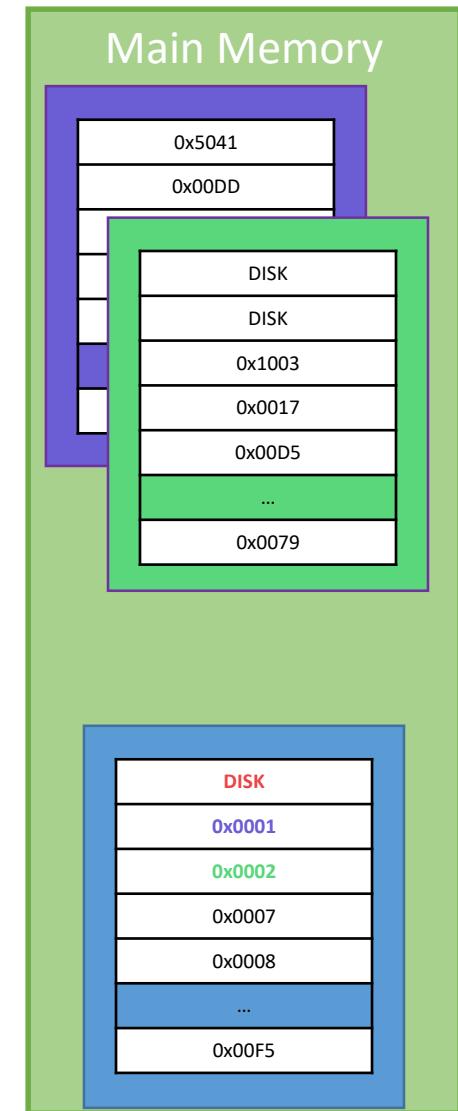
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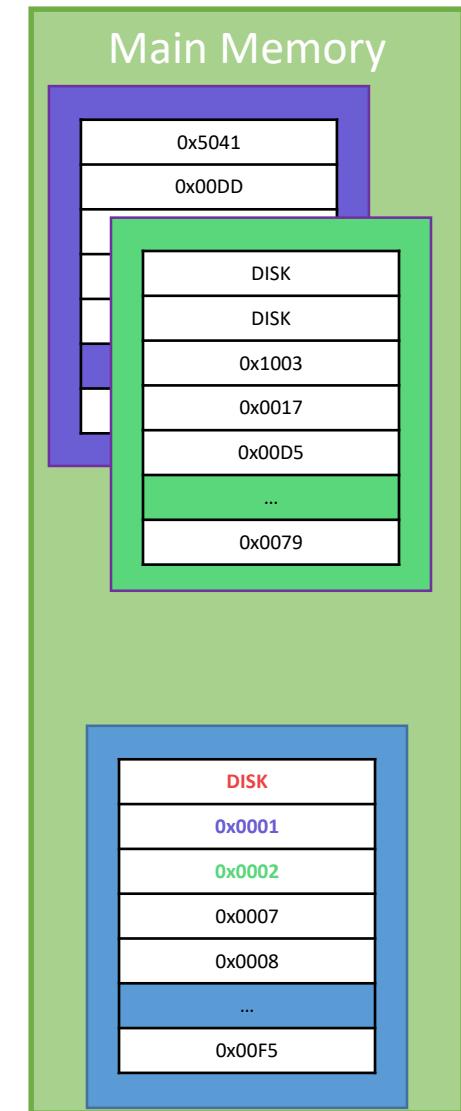
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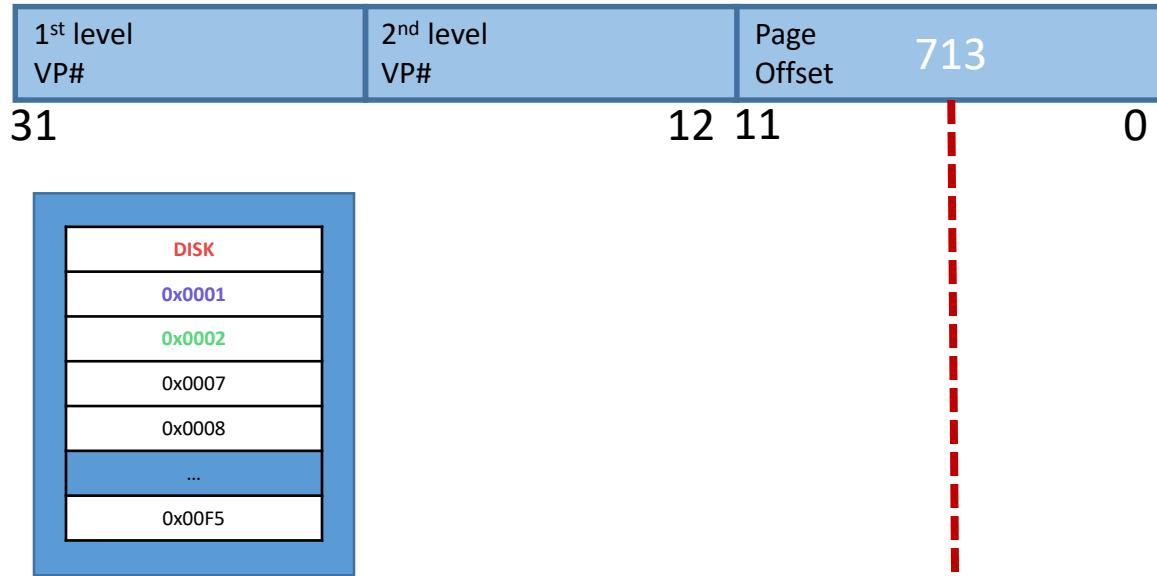


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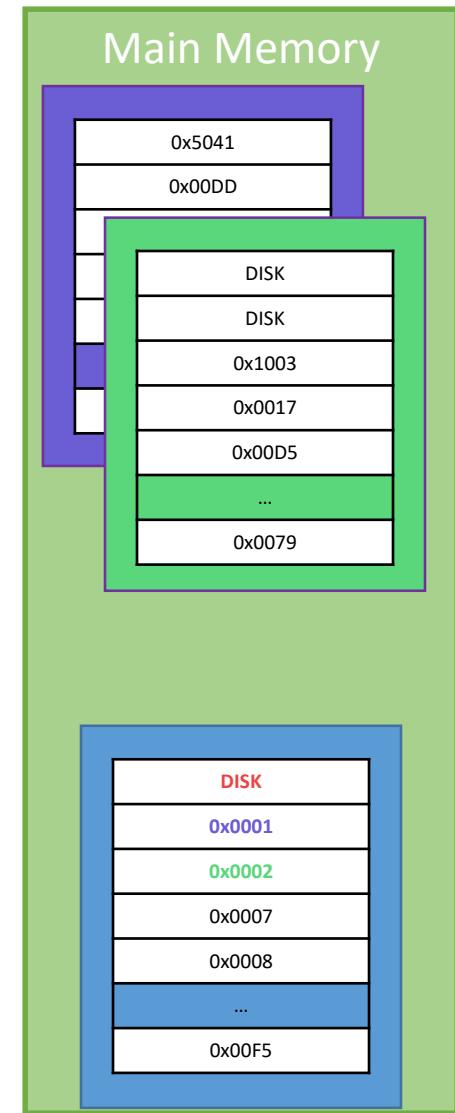
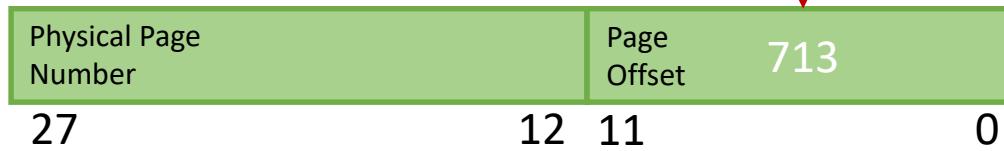
Multi-Level Page Table Translation

VA: 0x00403 713

Virtual Address [32 bit]



Physical Address [28 bits]

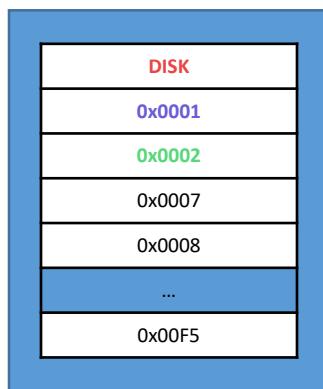


Quincy Flint

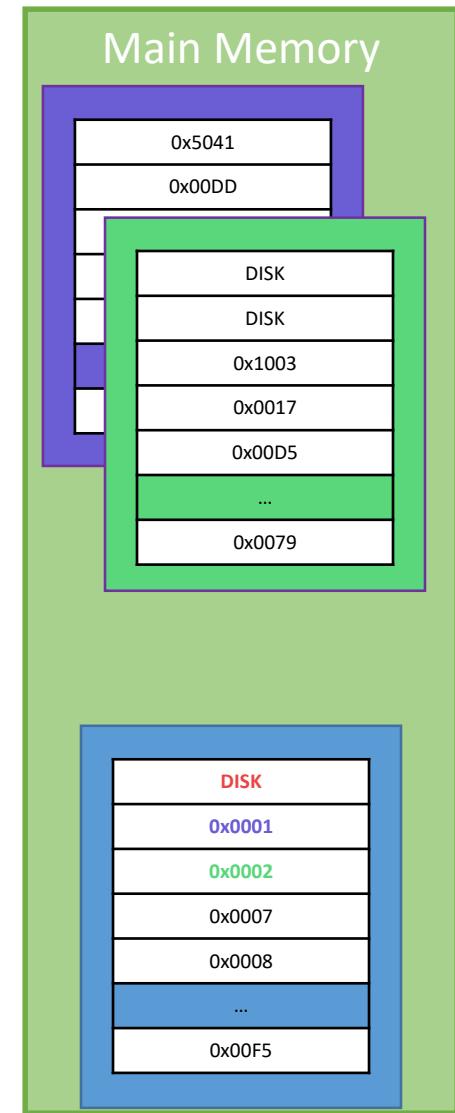
Multi-Level Page Table Translation

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Virtual Address [32 bit]



Physical Address [28 bits]

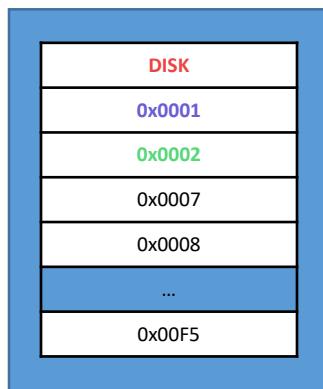
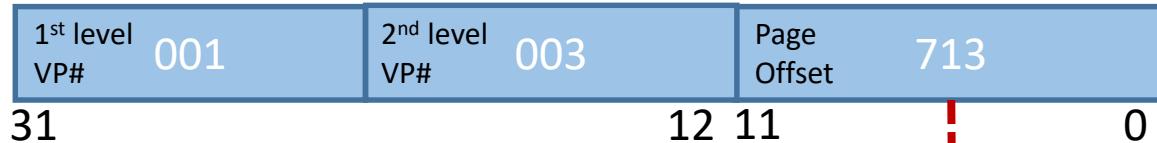


Quincy Flint

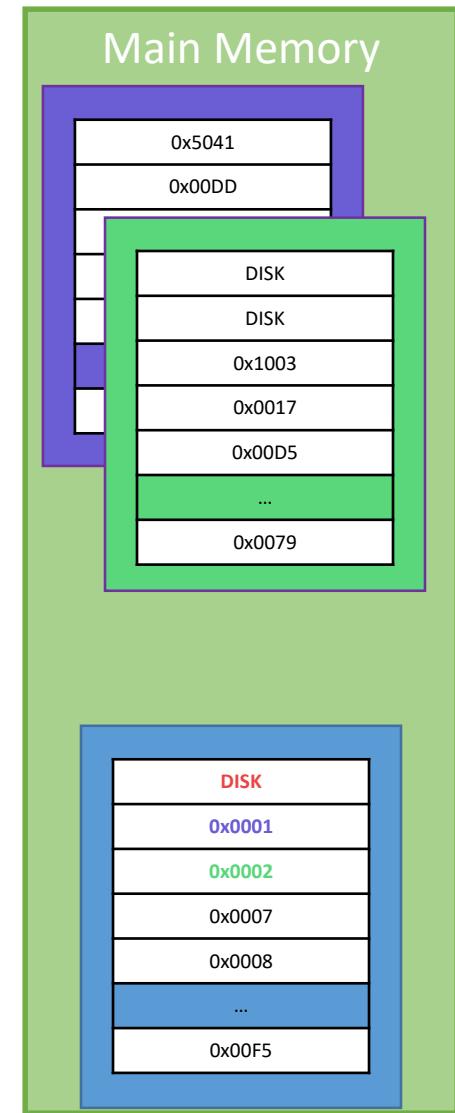
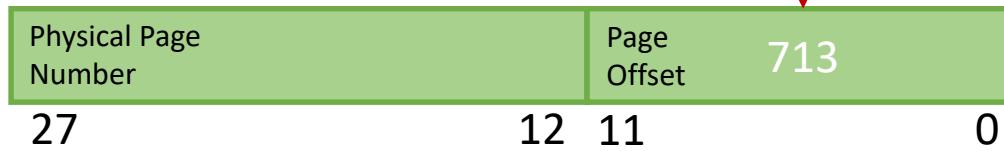
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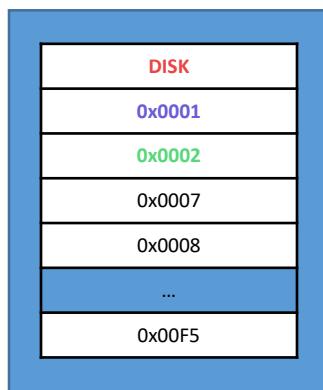
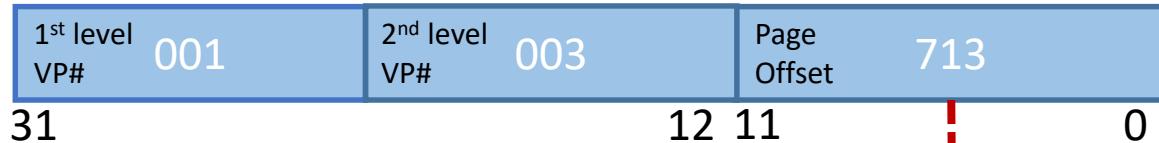


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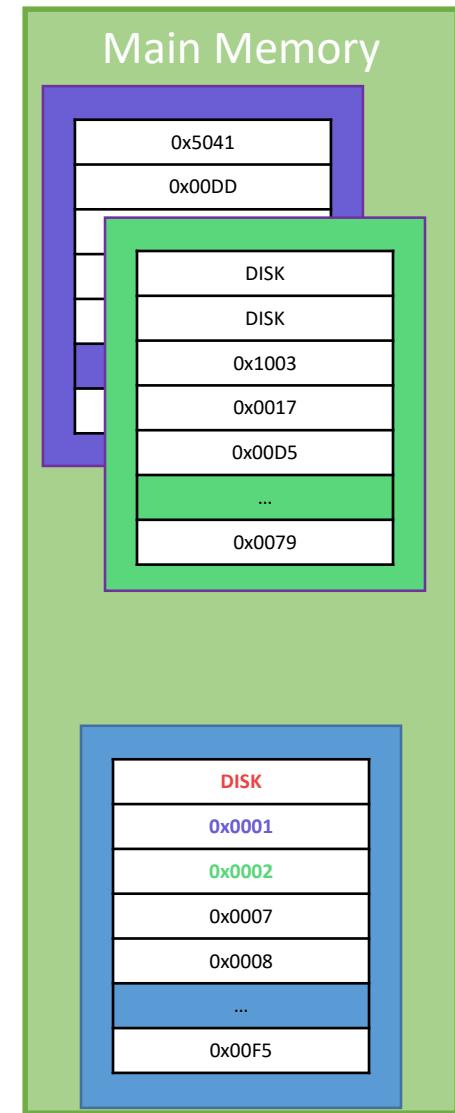
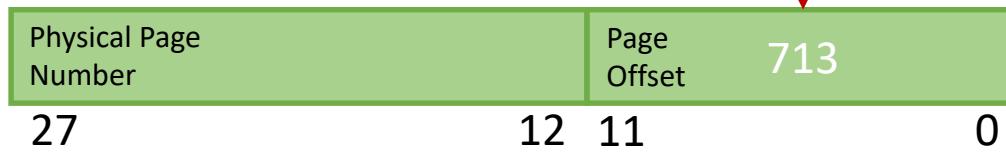
Multi-Level Page Table Translation

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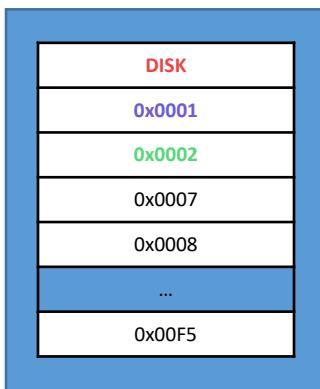
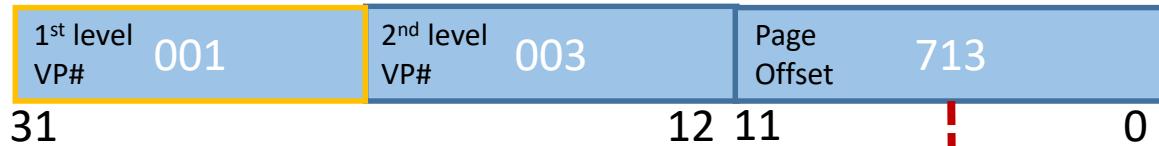


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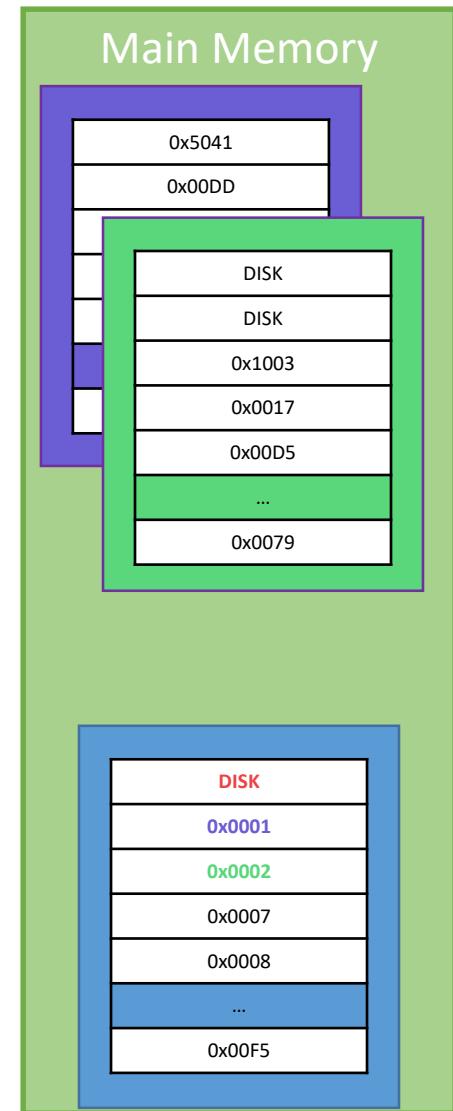
Multi-Level Page Table Translation

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Virtual Address [32 bit]



Physical Address [28 bits]

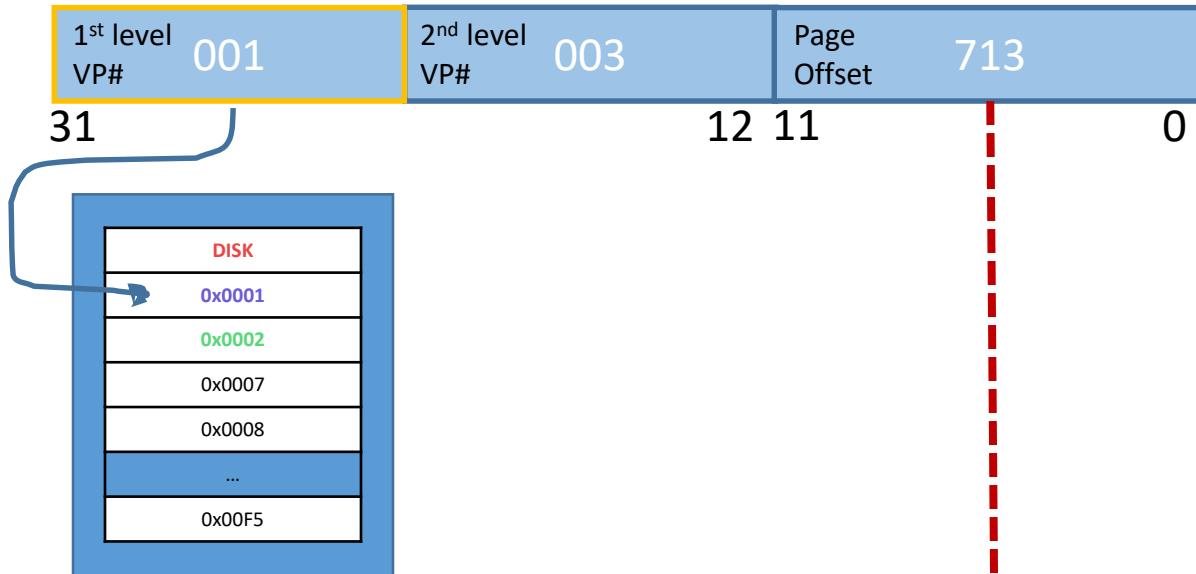


Quincy Flint

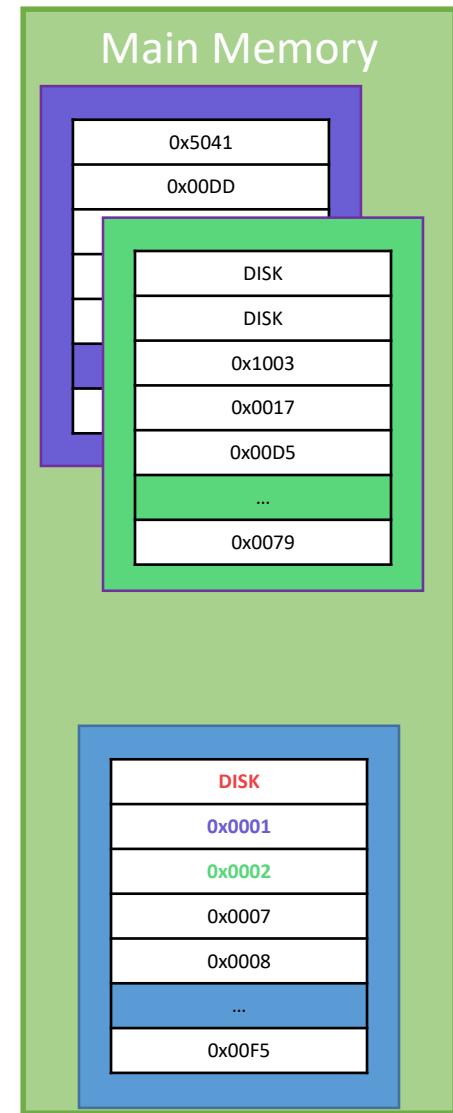
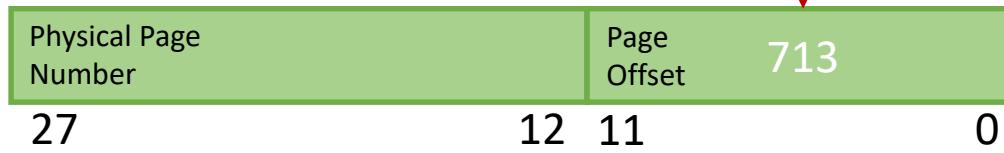
Multi-Level Page Table Translation

VA: 0x00403 713

Virtual Address [32 bit]



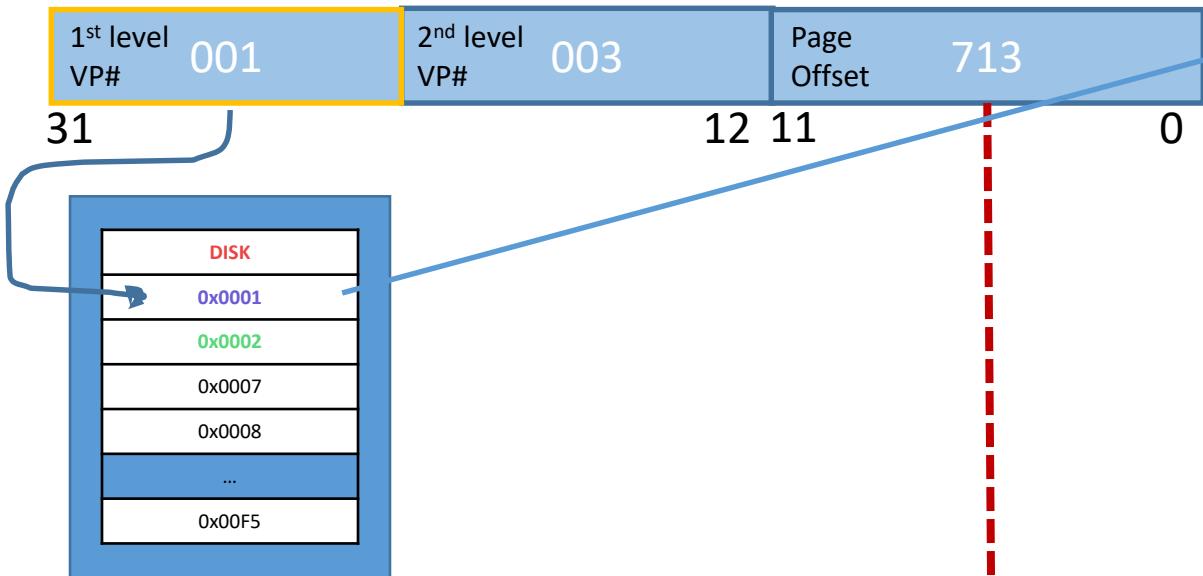
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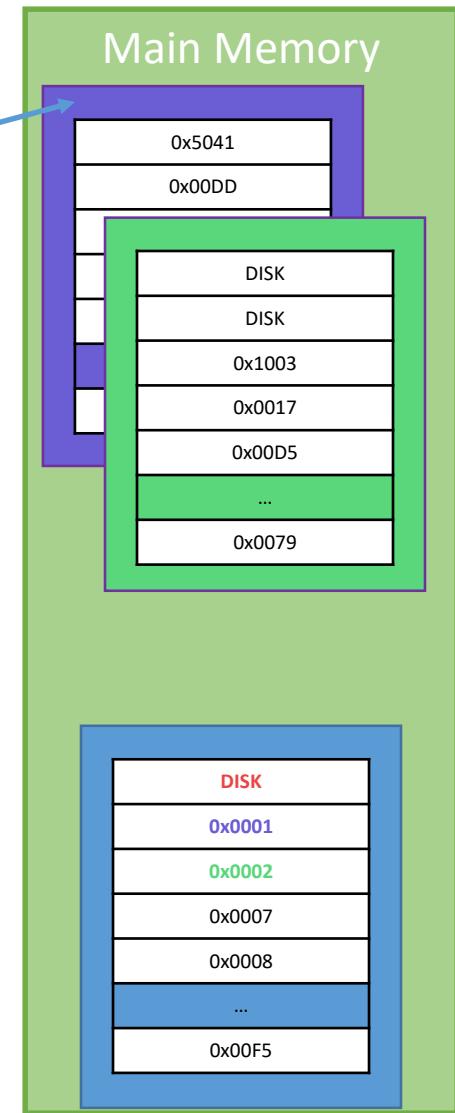
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Multi-Level Page Table Translation
VA: 0x00403 713

Virtual Address [32 bit]



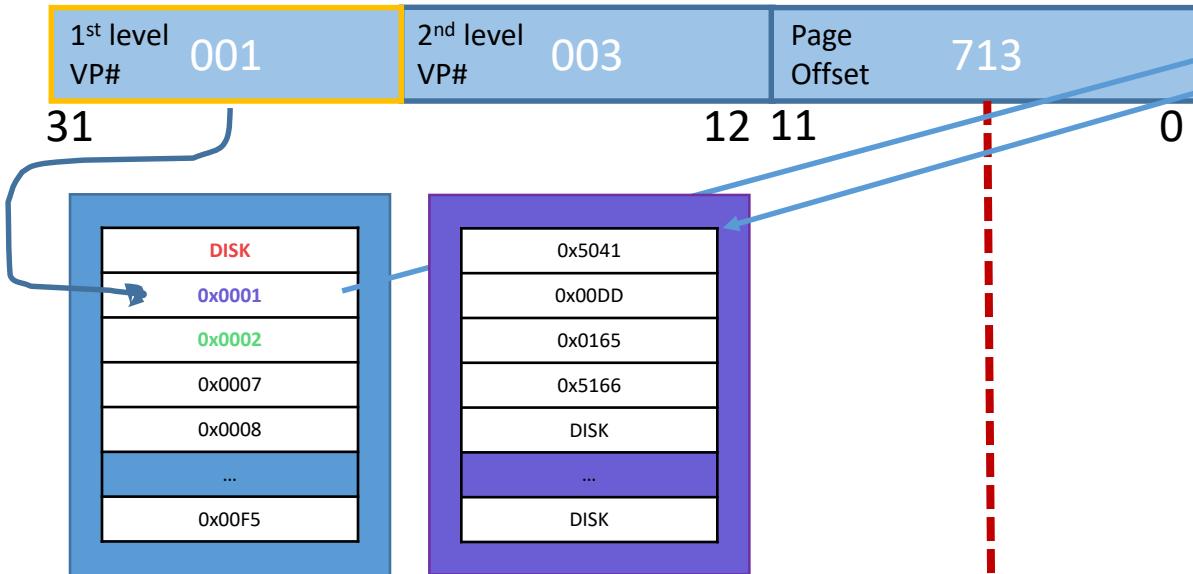
Physical Address [28 bits]



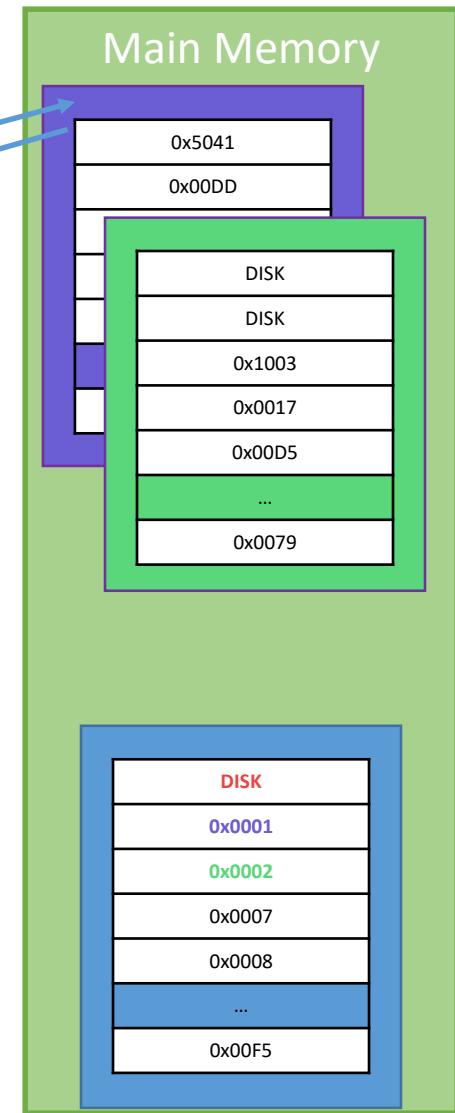
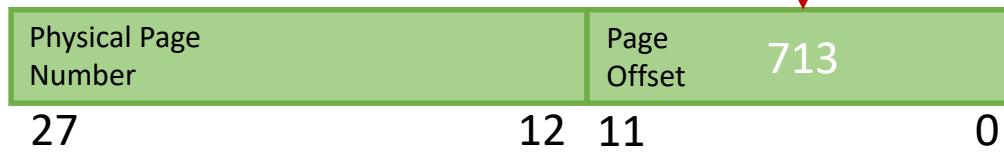
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Multi-Level Page Table Translation
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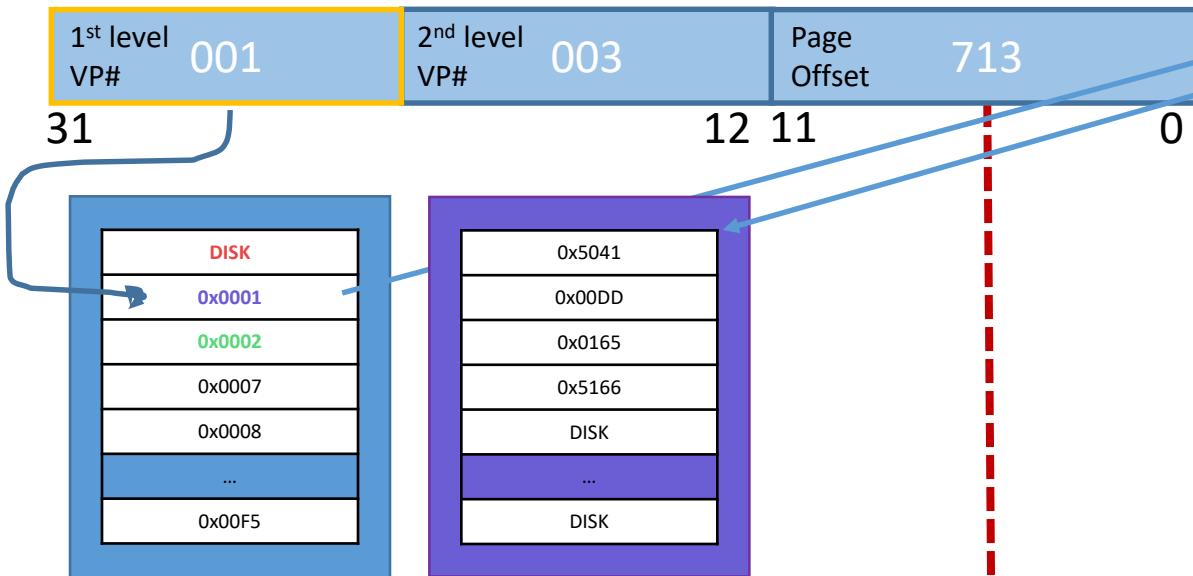
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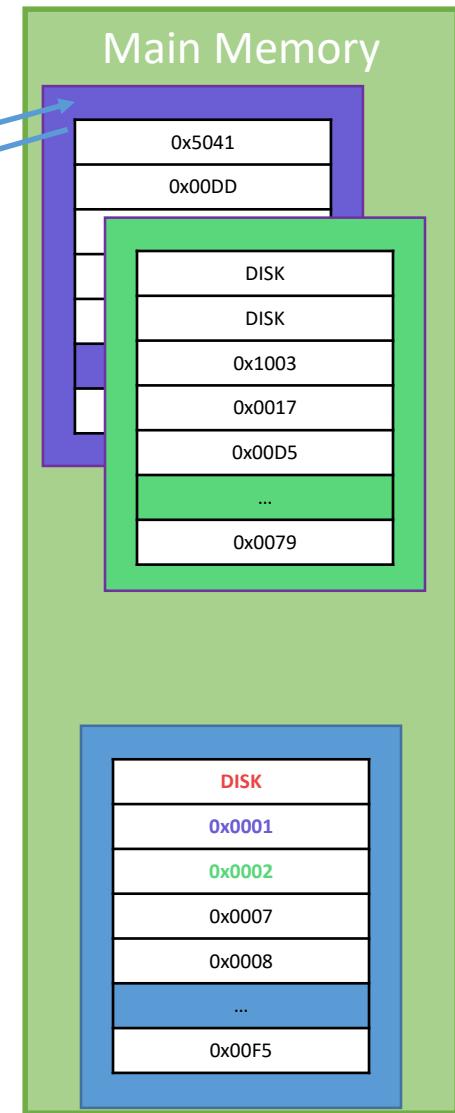
Quincy Flint

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Virtual Address [32 bit]



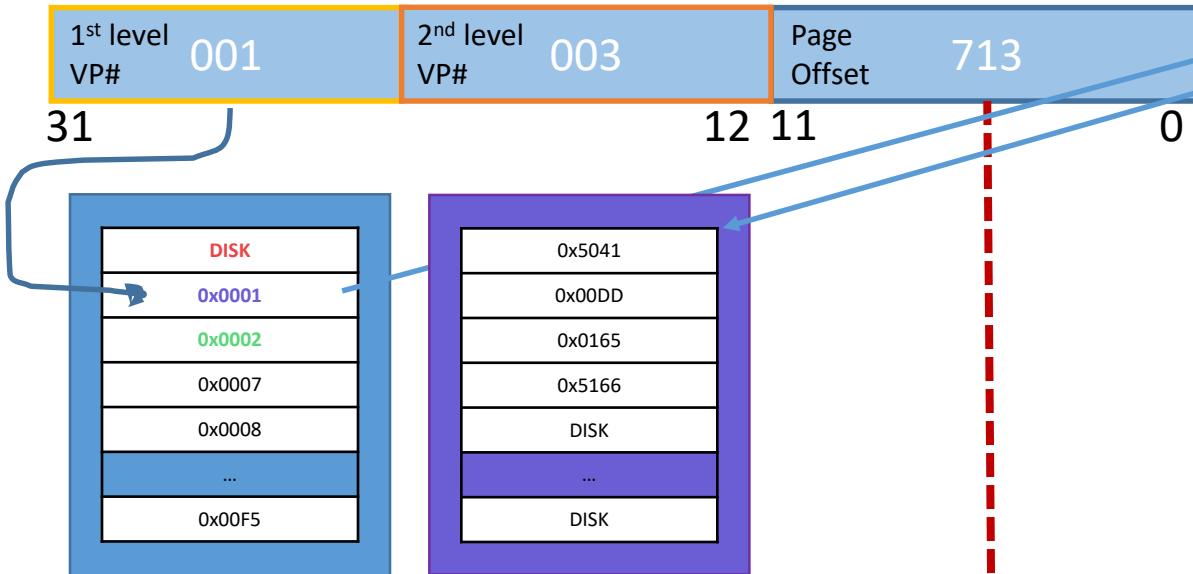
Physical Address [28 bits]



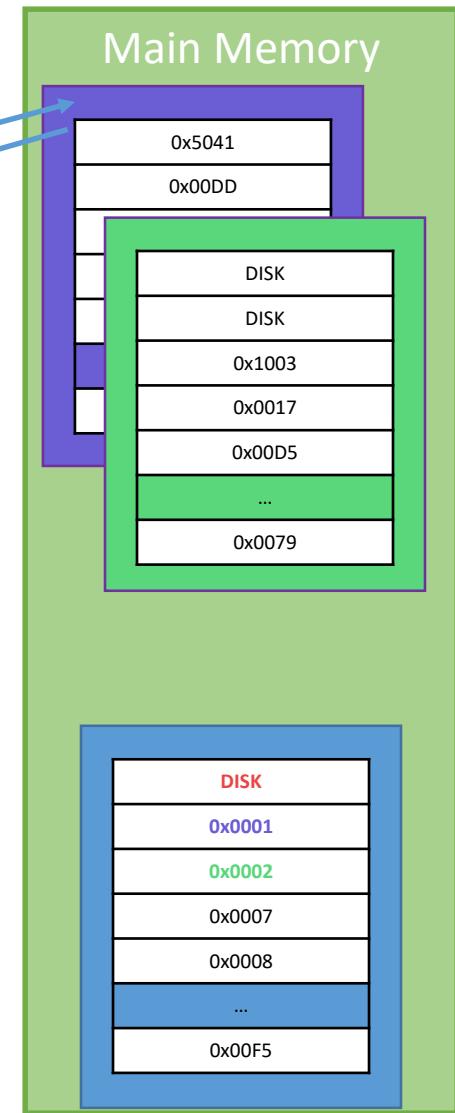
Quincy Flint

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Virtual Address [32 bit]



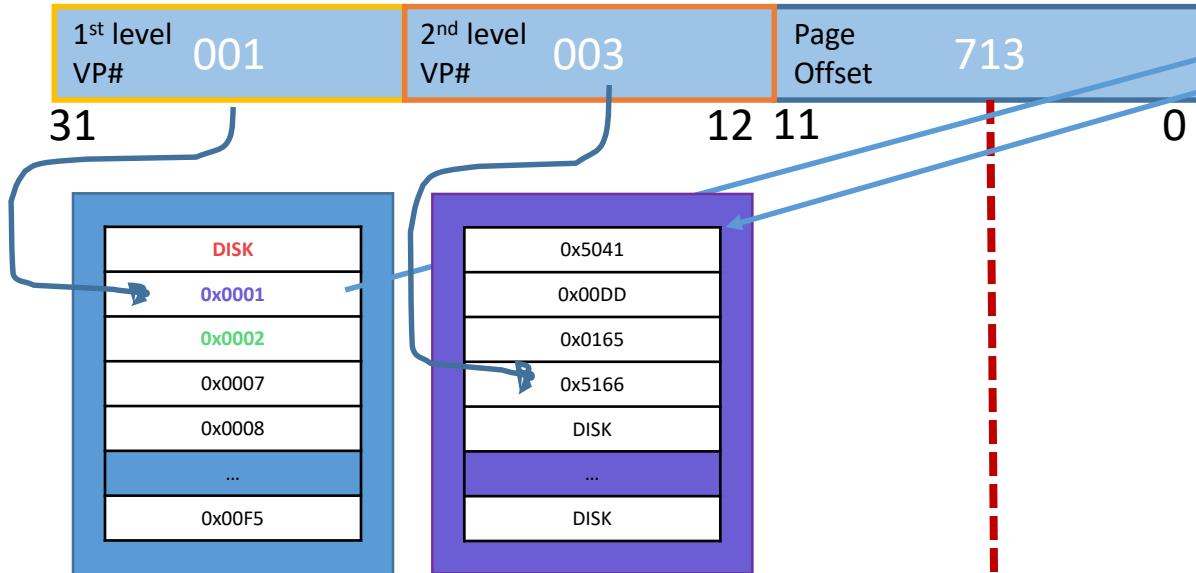
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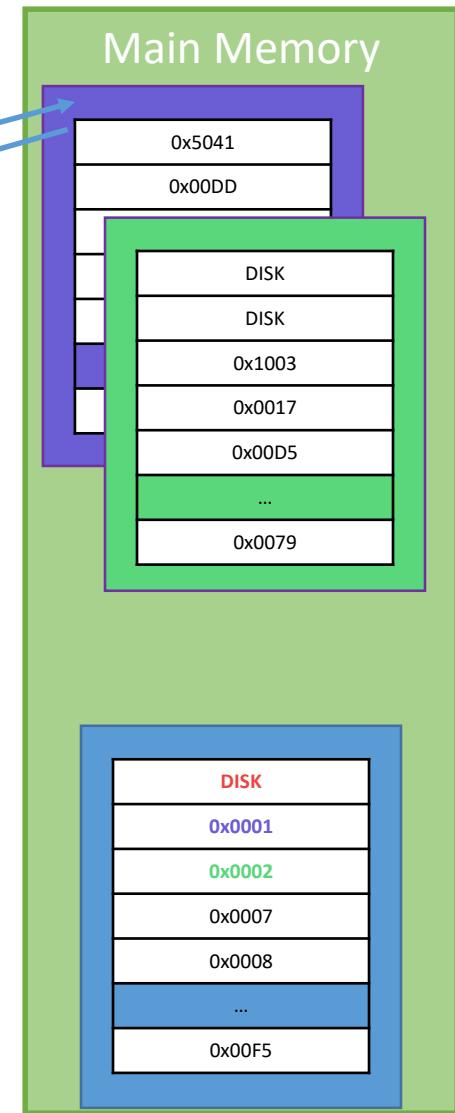
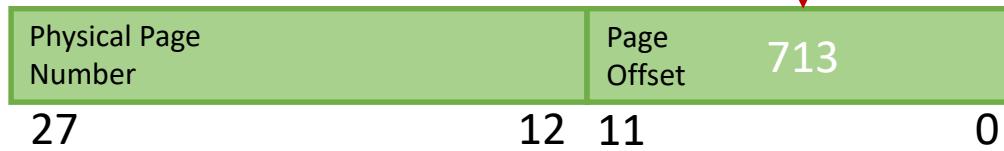
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Multi-Level Page Table Translation
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Virtual Address [32 bit]



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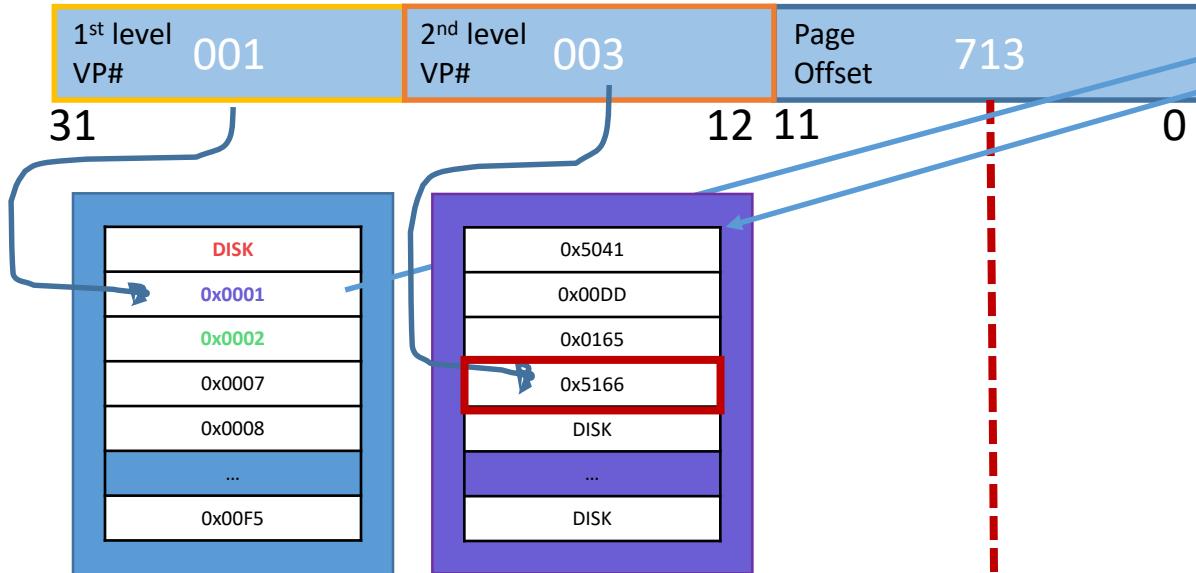


Quincy Flint

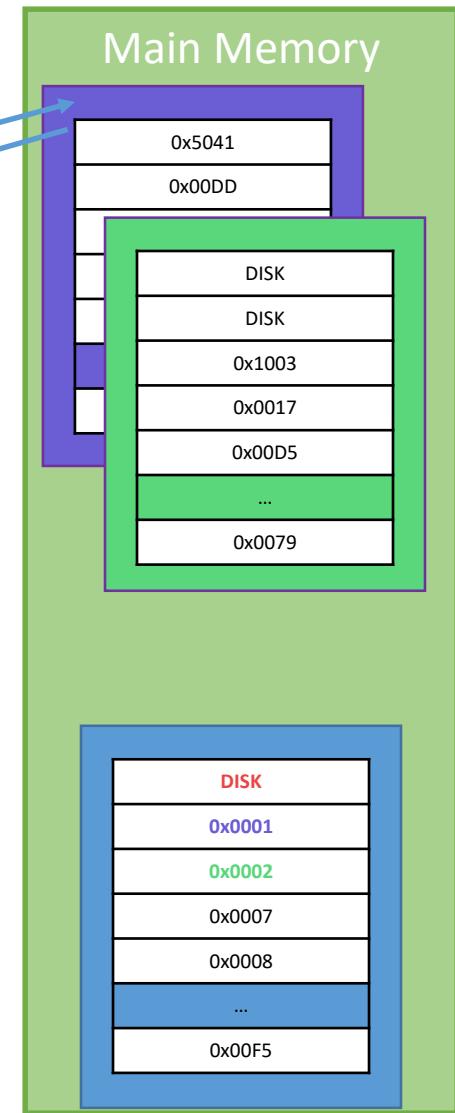
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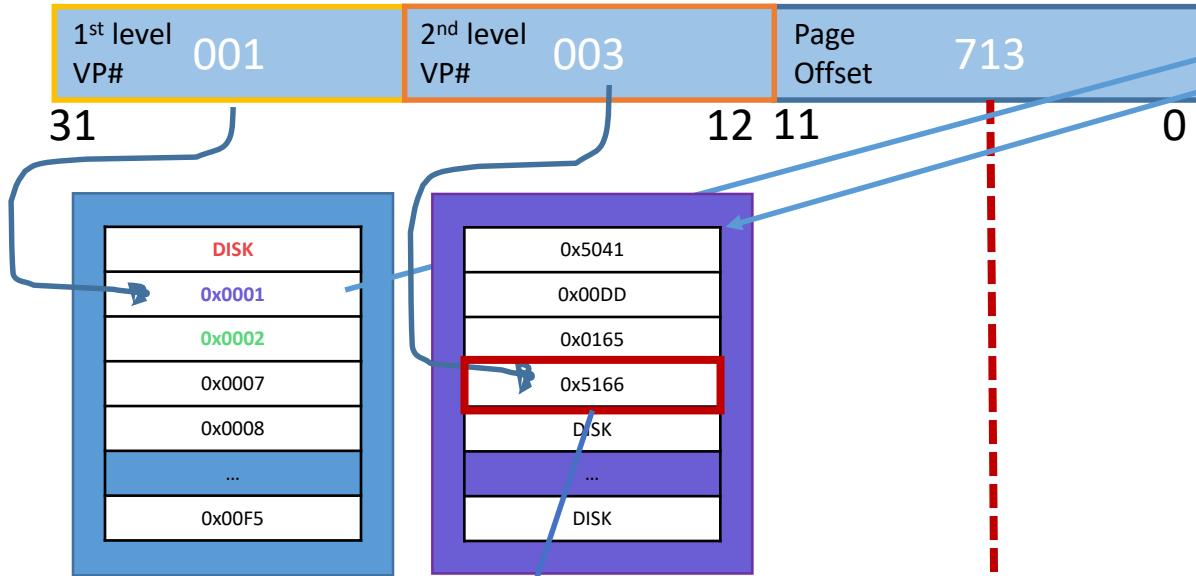


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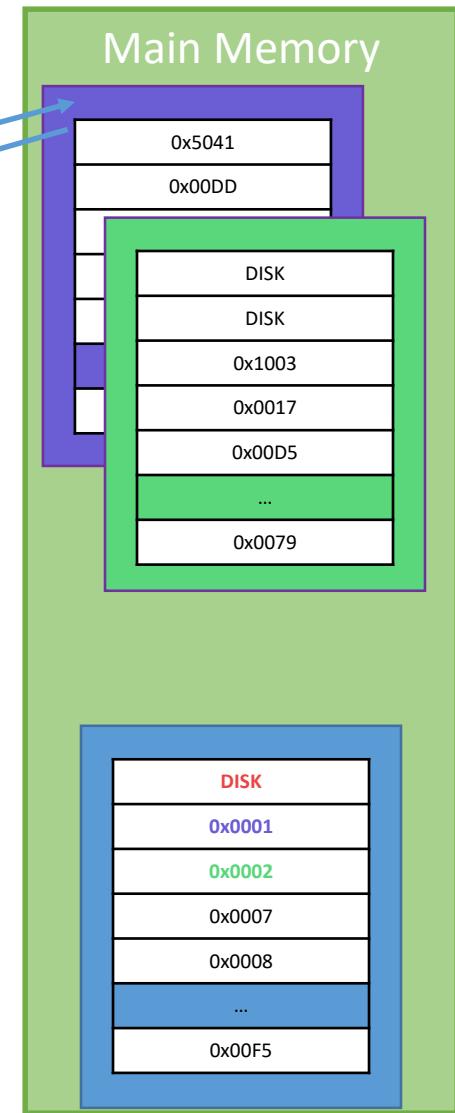
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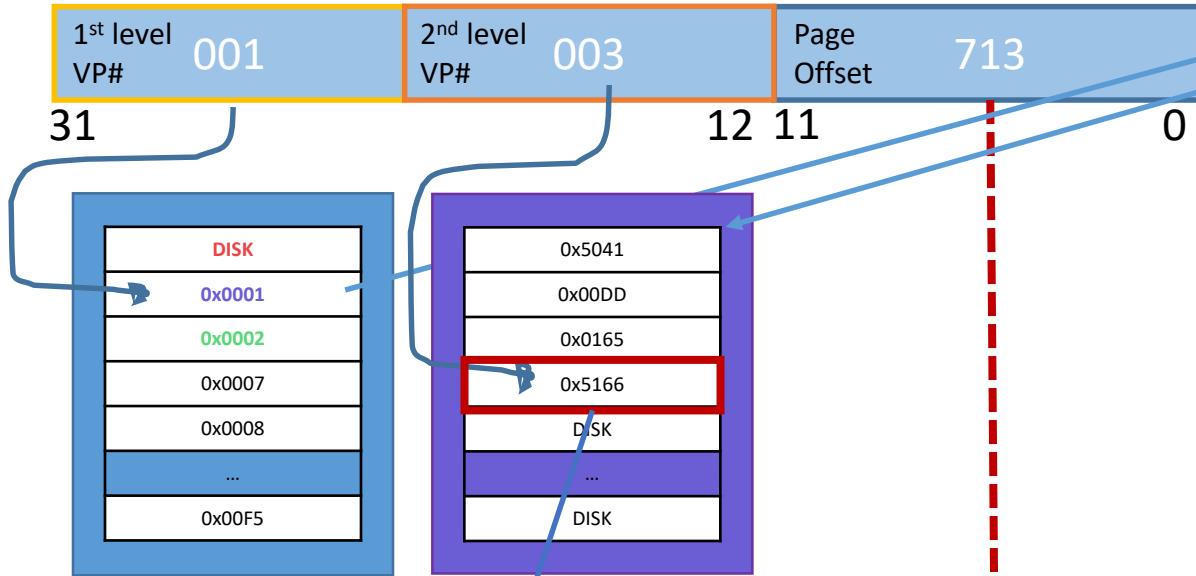


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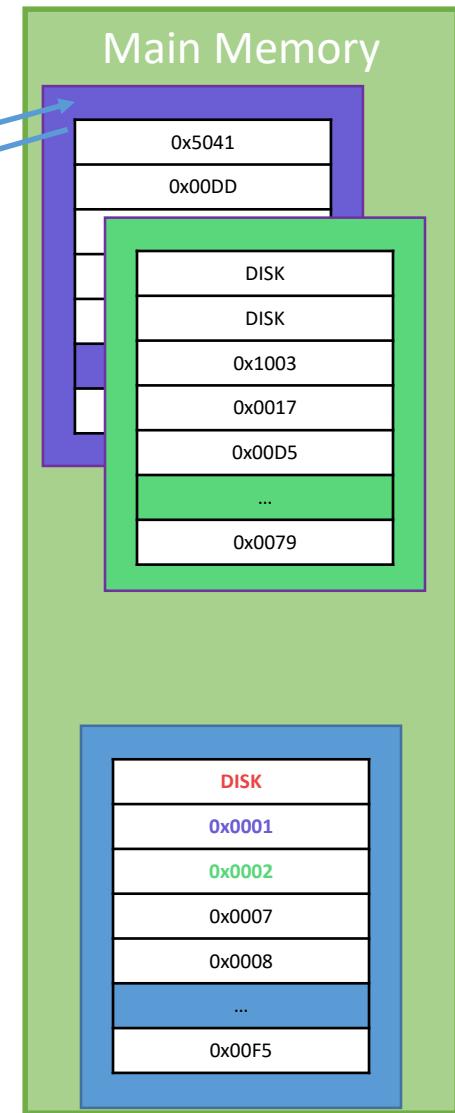
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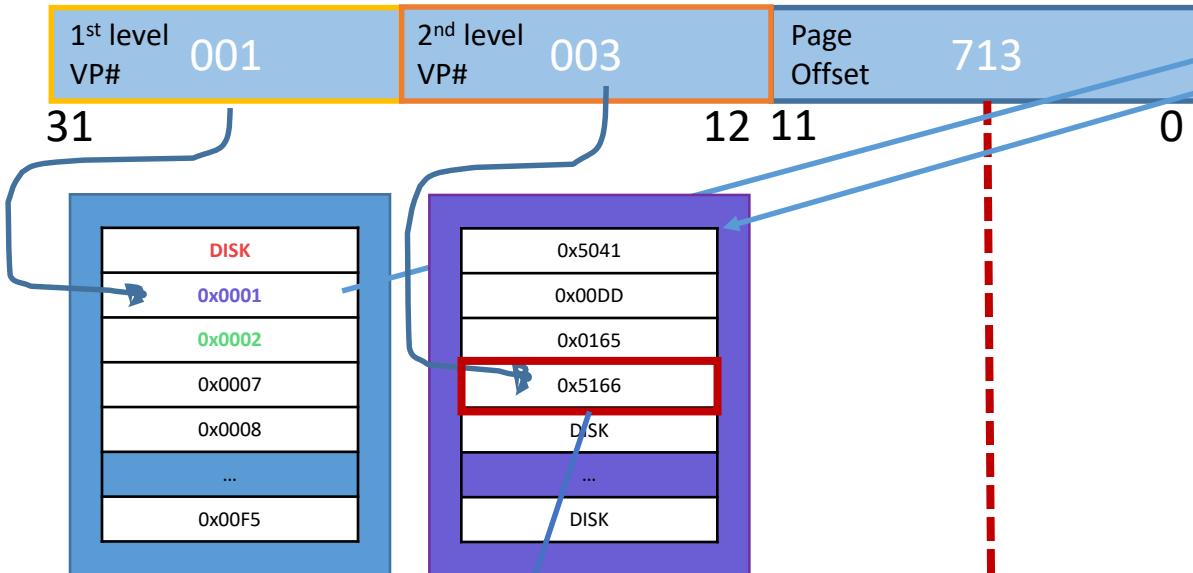
Physical Address [28 bits]



Quincy Flint

Multi-Level Page Table Translation
VA: 0x00403 713

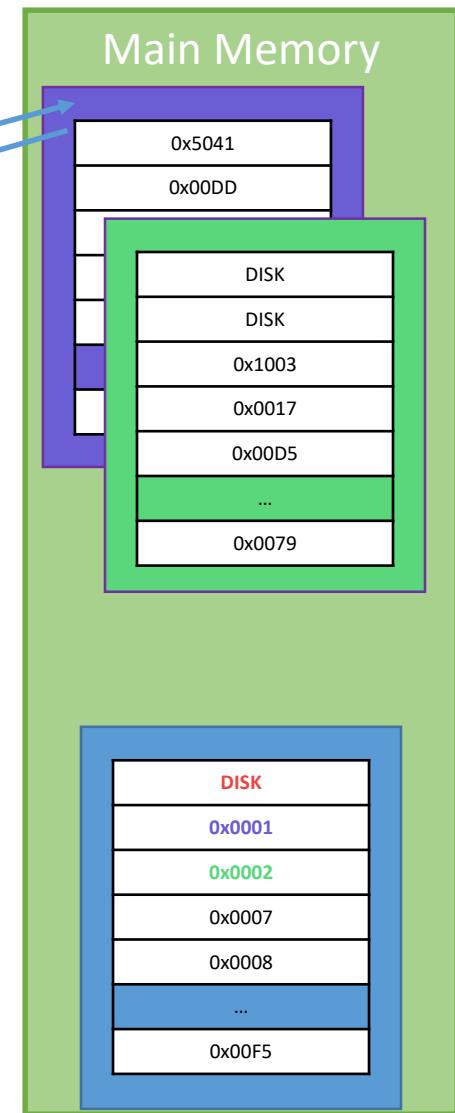
Virtual Address [32 bit]



Physical Address [28 bits]

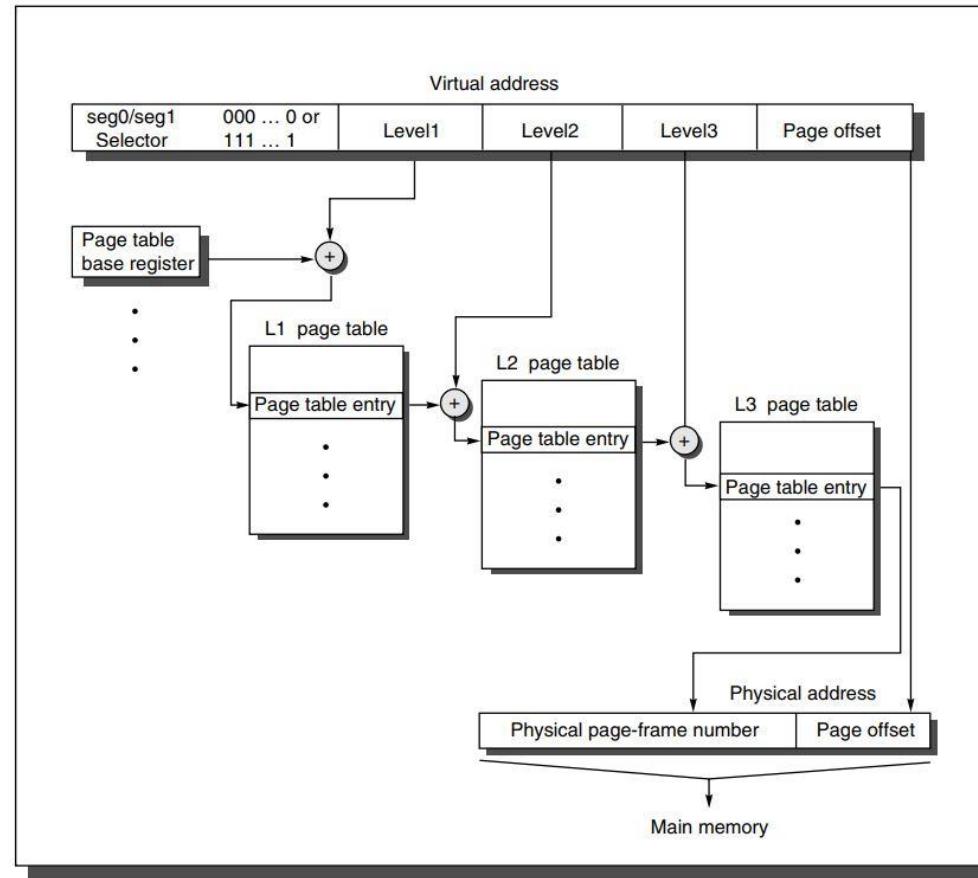


PA: 0x5166 713



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Illustration from the textbook (advanced)



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Multi-Level Page Table: Outro

- We always need to keep the 1st level Page Table in memory

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Multi-Level Page Table: Outro

- We always need to keep the 1st level Page Table in memory
- We need at least one 2nd level Page Table to do translations

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Multi-Level Page Table: Outro

- We always need to keep the 1st level Page Table in memory
- We need at least one 2nd level Page Table to do translations
- 2-Tier translation

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Multi-Level Page Table: Outro

- We always need to keep the 1st level Page Table in memory
- We need at least one 2nd level Page Table to do translations
- 2-Tier translation
 - Top-most **10** bits used to index **PT1**

Quincy Flint

Multi-Level Page Table: Outro

- We always need to keep the 1st level Page Table in memory
- We need at least one 2nd level Page Table to do translations
- 2-Tier translation
 - Top-most **10** bits used to index **PT1**
 - Middle-most **10** bits used to index **PT2**

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Multi-Level Page Table: Outro

- We always need to keep the 1st level Page Table in memory
- We need at least one 2nd level Page Table to do translations
- 2-Tier translation
 - Top-most **10** bits used to index **PT1**
 - Middle-most **10** bits used to index **PT2**
- Advantage:
 - We can now keep Page Tables on disk

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Multi-Level Page Table: Outro

- We always need to keep the 1st level Page Table in memory
- We need at least one 2nd level Page Table to do translations
- 2-Tier translation
 - Top-most **10** bits used to index **PT1**
 - Middle-most **10** bits used to index **PT2**
- Advantage:
 - We can now keep Page Tables on disk
 - We can still address the same amount of data

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Quiz: Multi-Level Page Tables



Q: With multilevel page tables, if I am running *100* applications *concurrently*, how much memory do I need in RAM?

- I. 4 kB
- II. 8 kB
- III. 8 MB
- IV. 800 kB
- V. 400 MB

Quincy Flint

Quiz: Multi-Level Page Tables

Q: With multilevel page tables, if I am running *100* applications *concurrently*, how much memory do I need in RAM?

- I. 4 kB
- II. 8 kB
- III. 8 MB
- IV. 800 kB
- V. 400 MB

A:

- IV. 800 kB

For each program, we must always keep the 1st level page table in RAM (4 kB) and we need at least one 2nd level page table to address data.

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Quiz: Multi-Level Page Tables



Q: Without multilevel page tables, if I am running *100* applications *concurrently*, how much memory do I need in RAM?

- I. 4 kB
- II. 8 kB
- III. 8 MB
- IV. 800 kB
- V. 400 MB

Quincy Flint

Quiz: Multi-Level Page Tables

Q: Without multilevel page tables, if I am running *100* applications *concurrently*, how much memory do I need in RAM?

- I. 4 kB
- II. 8 kB
- III. 8 MB
- IV. 800 kB
- V. 400 MB

A:

- IV. 400 MB

For each program, we must keep the entire 4 MB Page Table in RAM at all times.

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Inverted Page Tables

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References Quincy Flint

- David Black-Schaffer: Lecture Series on Virtual Memory
- Patterson, Hennessy: Computer Organization and Design: the Hardware/Software Interface
- Intel Hardware Data-Sheets
- Linux: Anatomy of a Program in Memory