Quincy Flint

Virtual Memory

EEL 3713C: Digital Computer Architecture

Quincy Flint

[Ionospheric Radio Lab in NEB]

Outline

1. Memory Problems
   - Not enough memory
   - Holes in address space
   - Programs overwriting
2. What is Virtual Memory?
   - Layer of indirection
   - How does indirection solve above
   - Page tables and translation
3. How do we implement VM?
   - Create and store page tables
   - Fast address translation
4. Virtual Memory and Caches
   - Prevent cache performance degradation when using VM

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Page Faults

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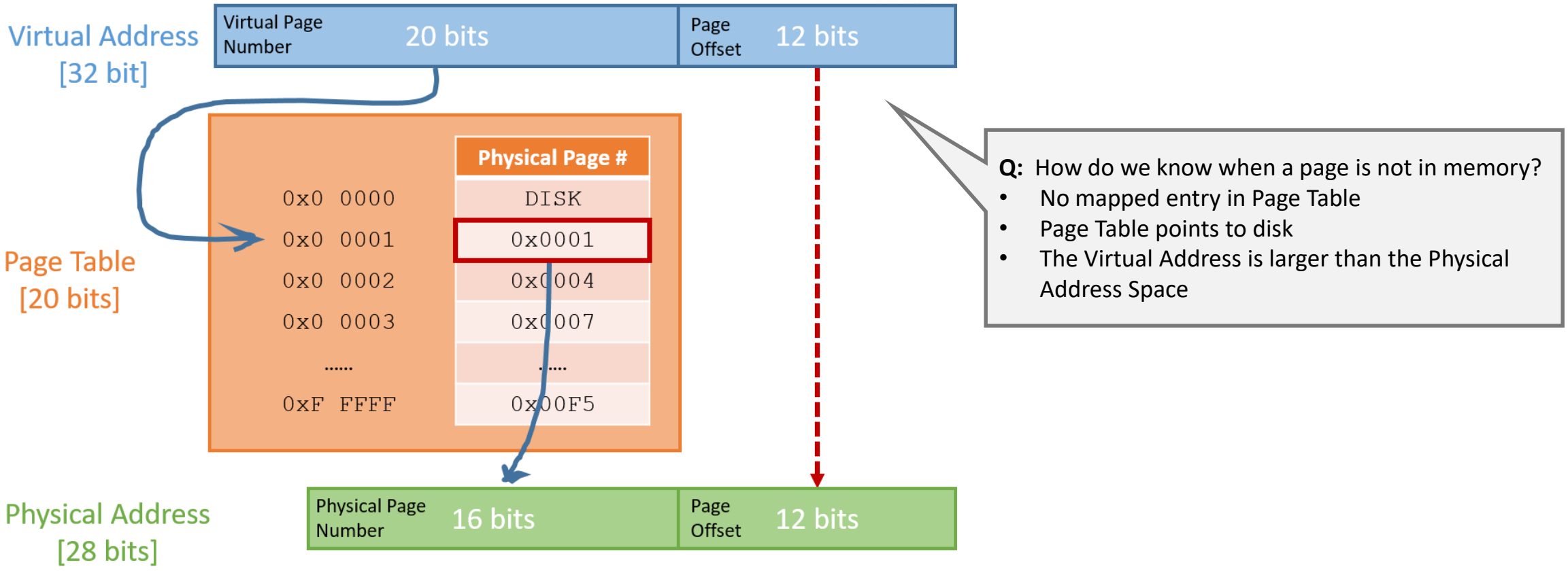
- A Page Fault occurs when we must access the disk to fetch data because it is not stored in memory.

What happens if a page is not in memory?



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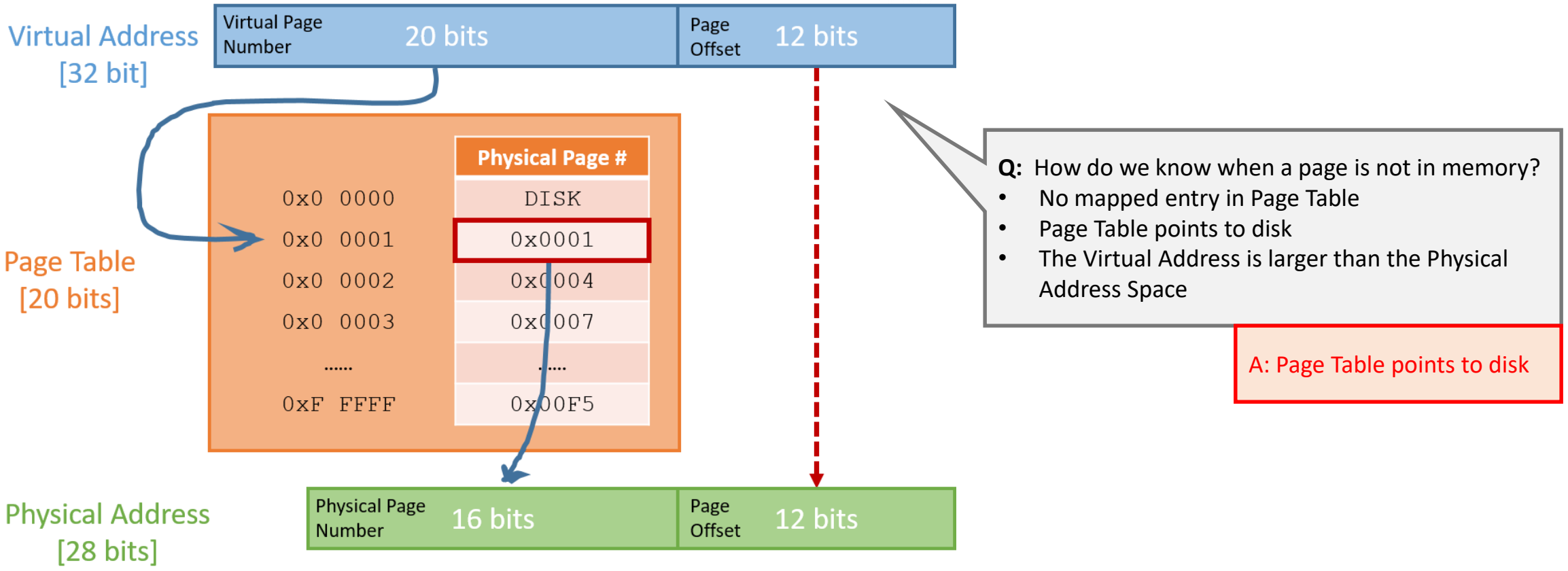

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Illustration from the textbook

Memory technology	Typical access time	$ per GIB in 2012
SRAM semiconductor memory	0.5–2.5 ns	$500–$1000
DRAM semiconductor memory	50–70 ns	$10–$20
Flash semiconductor memory	5,000–50,000 ns	$0.75–$1.00
Magnetic disk	5,000,000–20,000,000 ns	$0.05–$0.10

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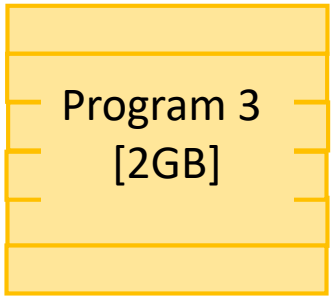
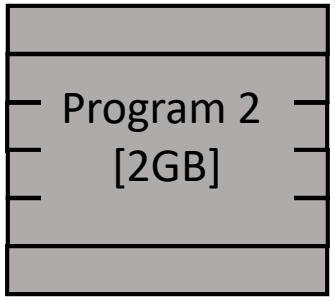
Memory Protection

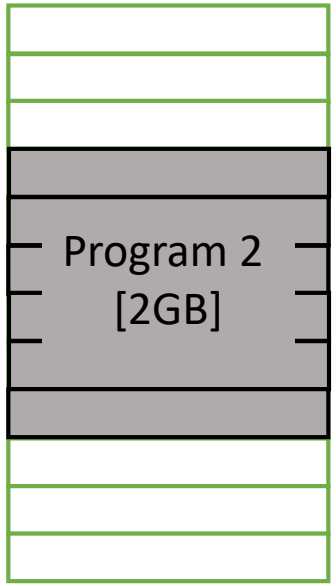
Virtual Memory Protects Applications *(Review)*

- Each program has its own Page Table. A program's Virtual Address is mapped to a unique Physical Address in memory.





4 GB [32-bit] RAM
Physical Address Space



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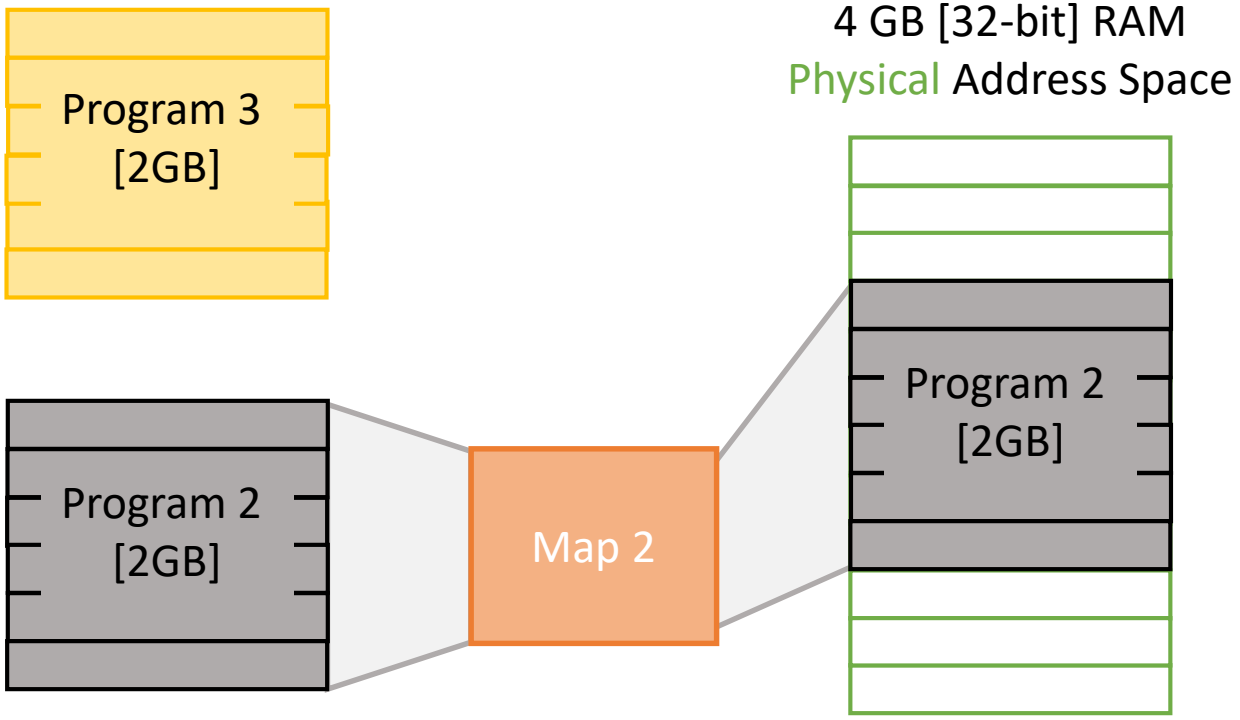

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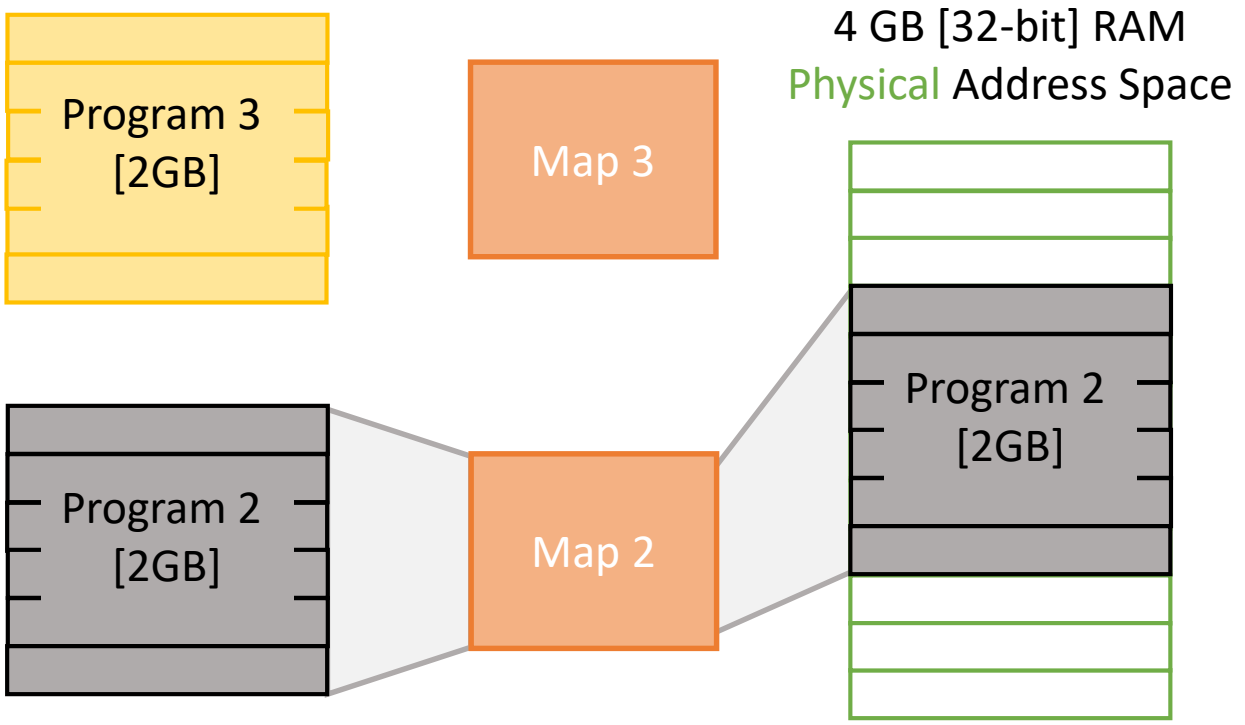

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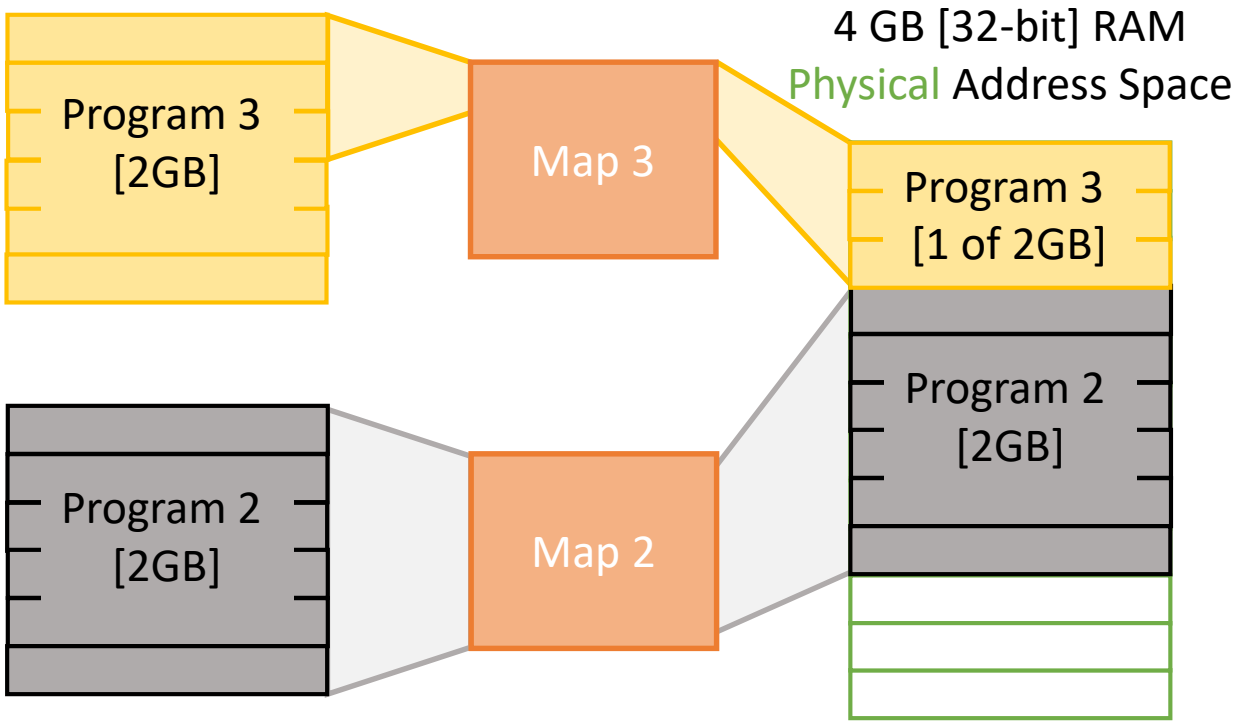

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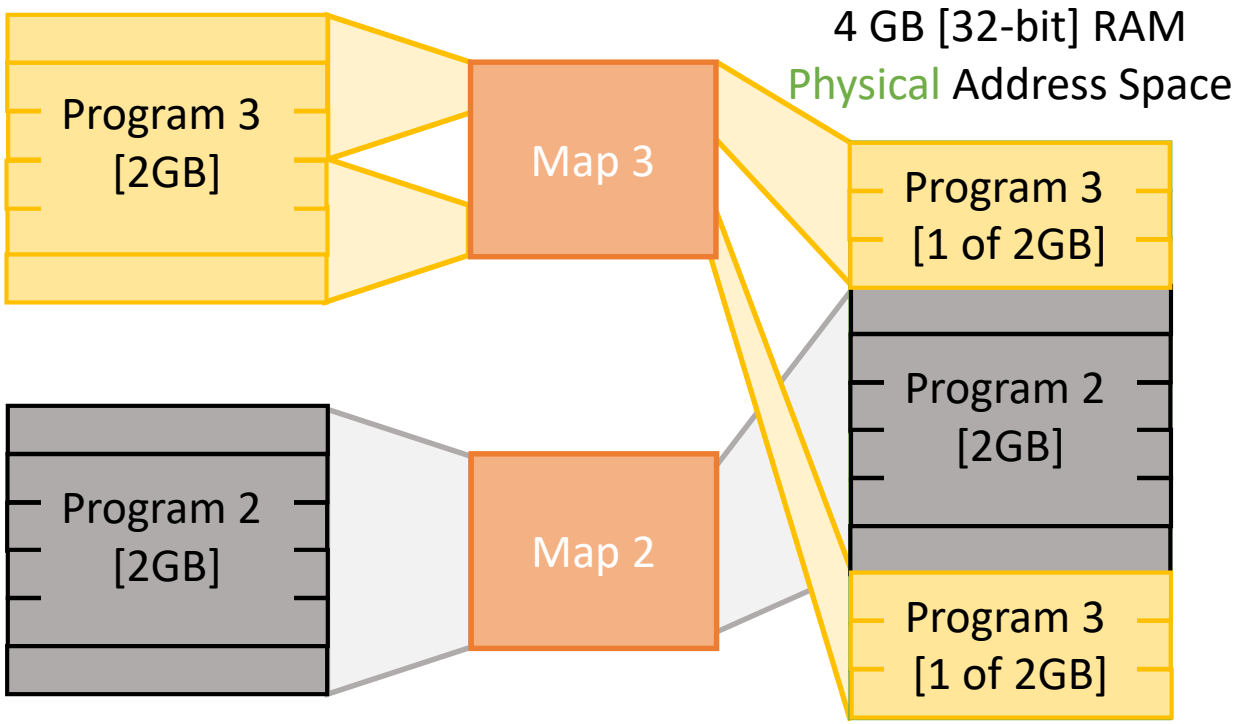

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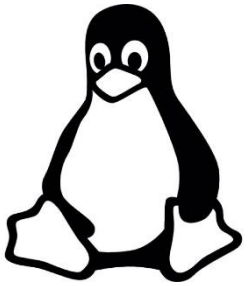
Linux Virtual Address Space



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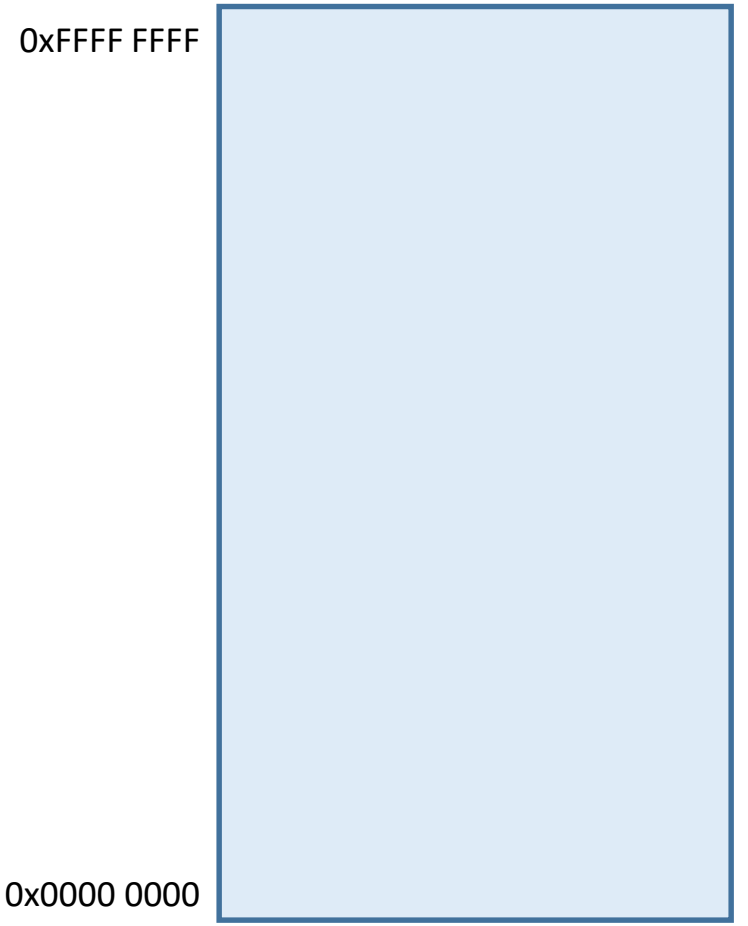

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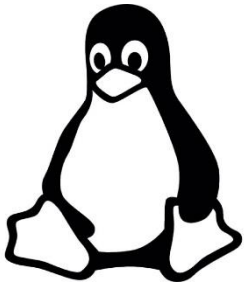

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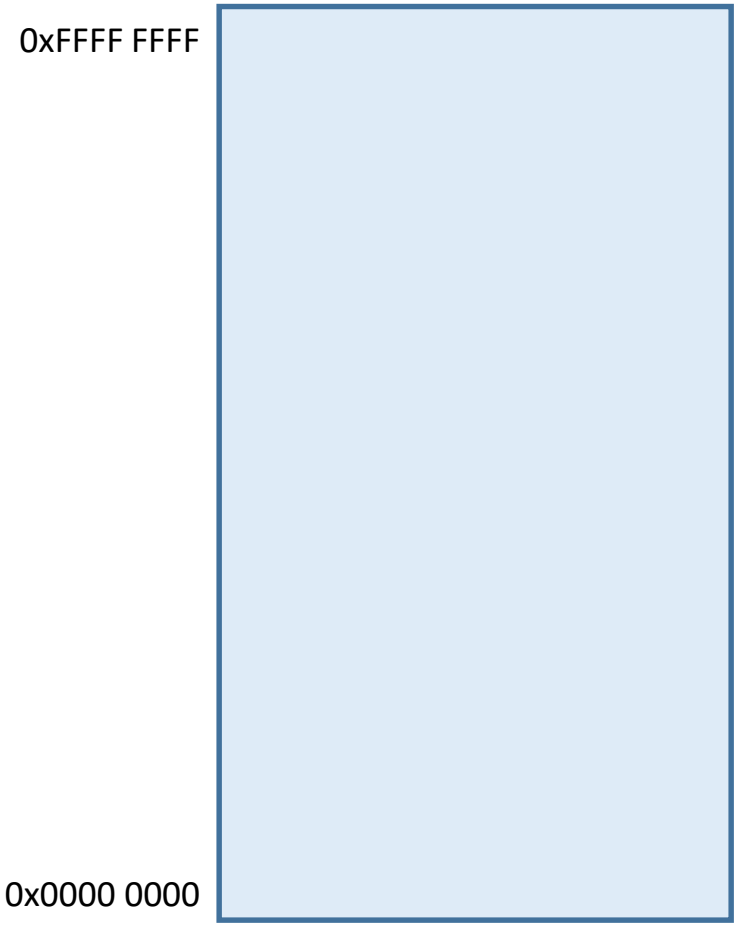
- The Linux Address Space -->



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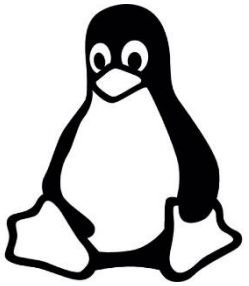

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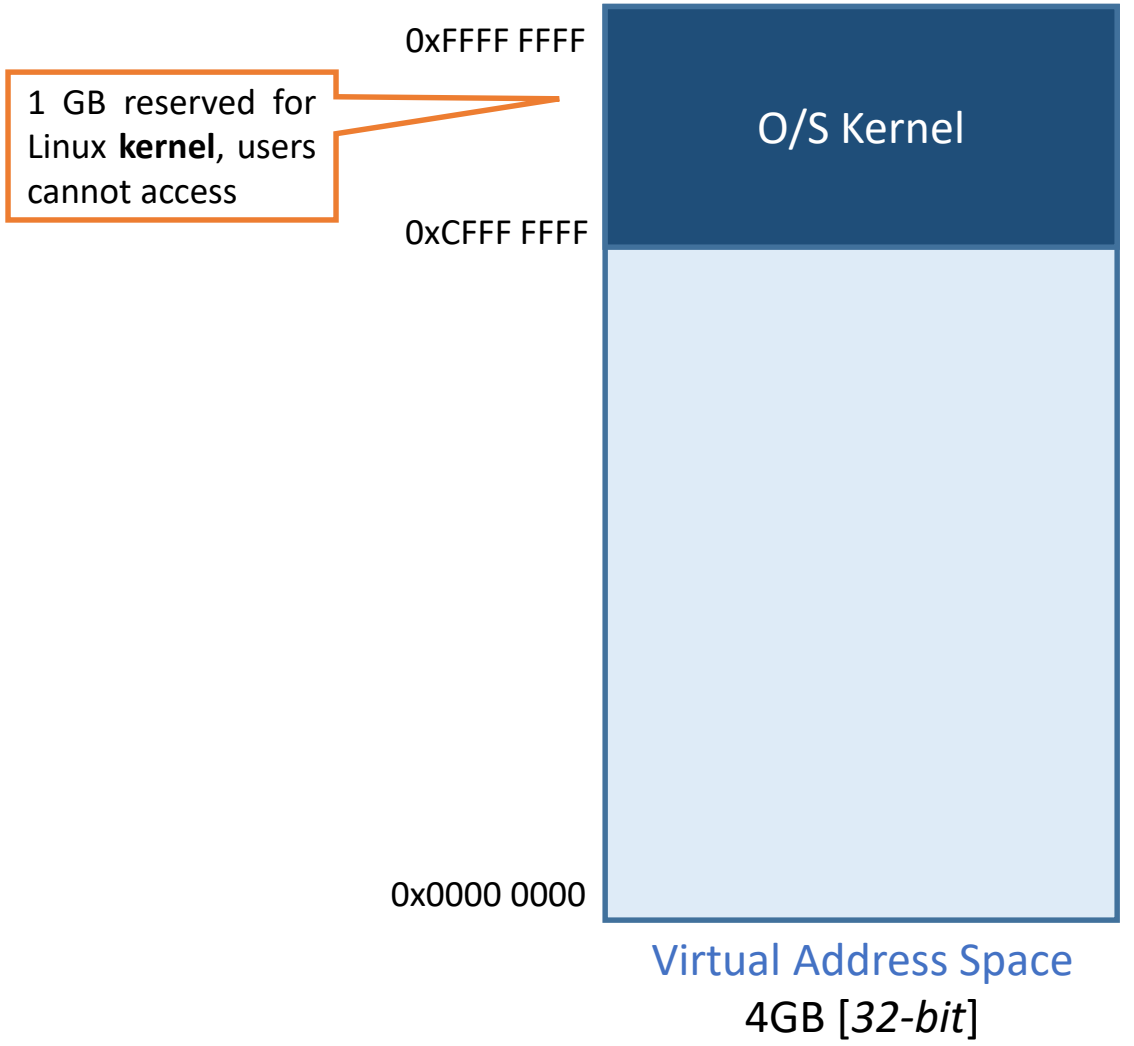

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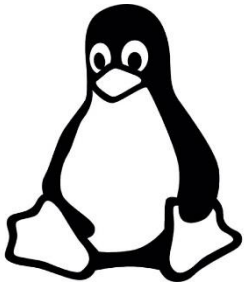

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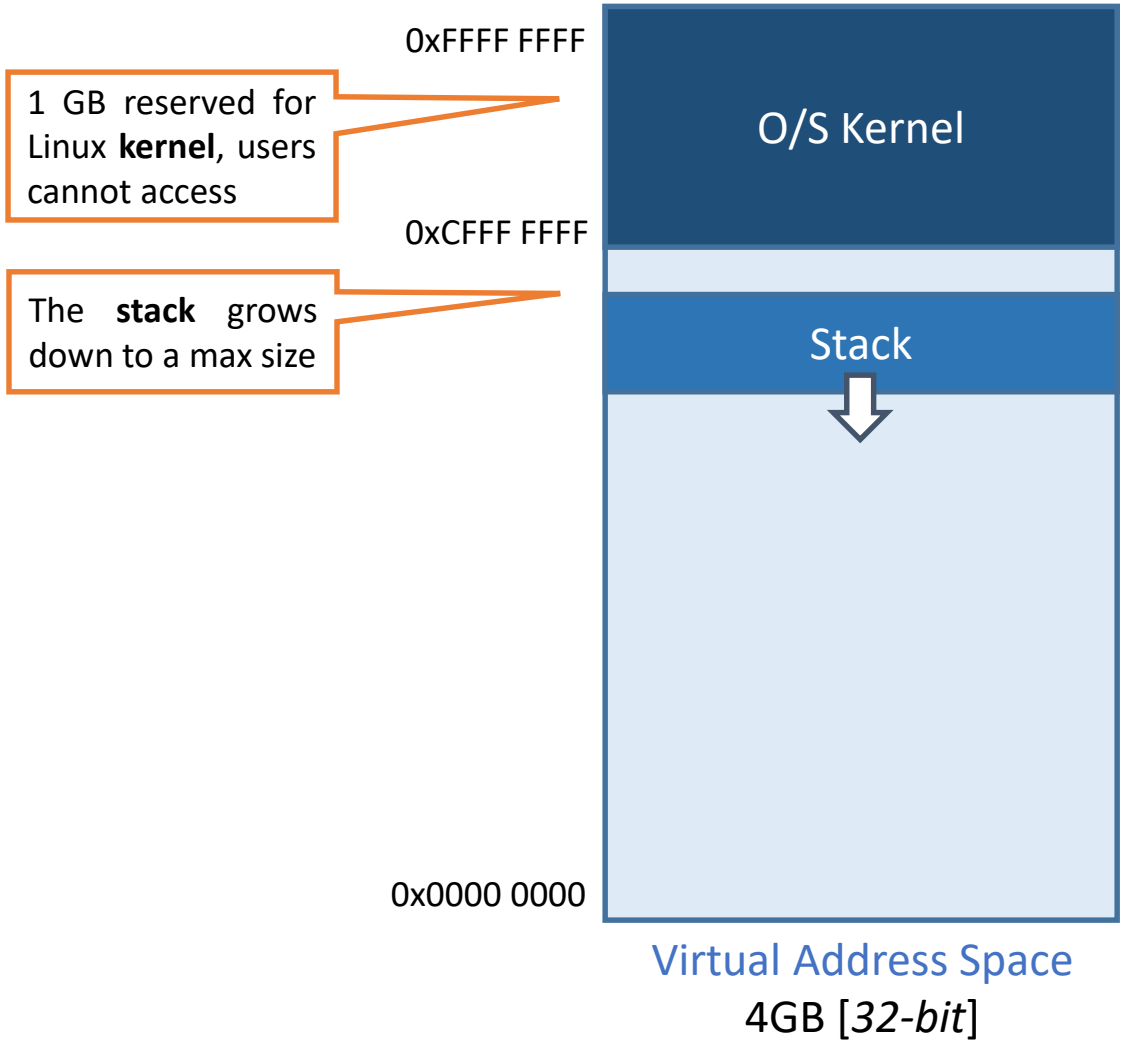

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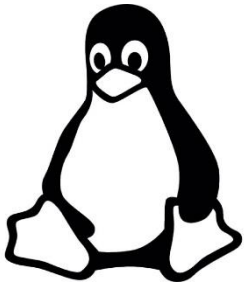

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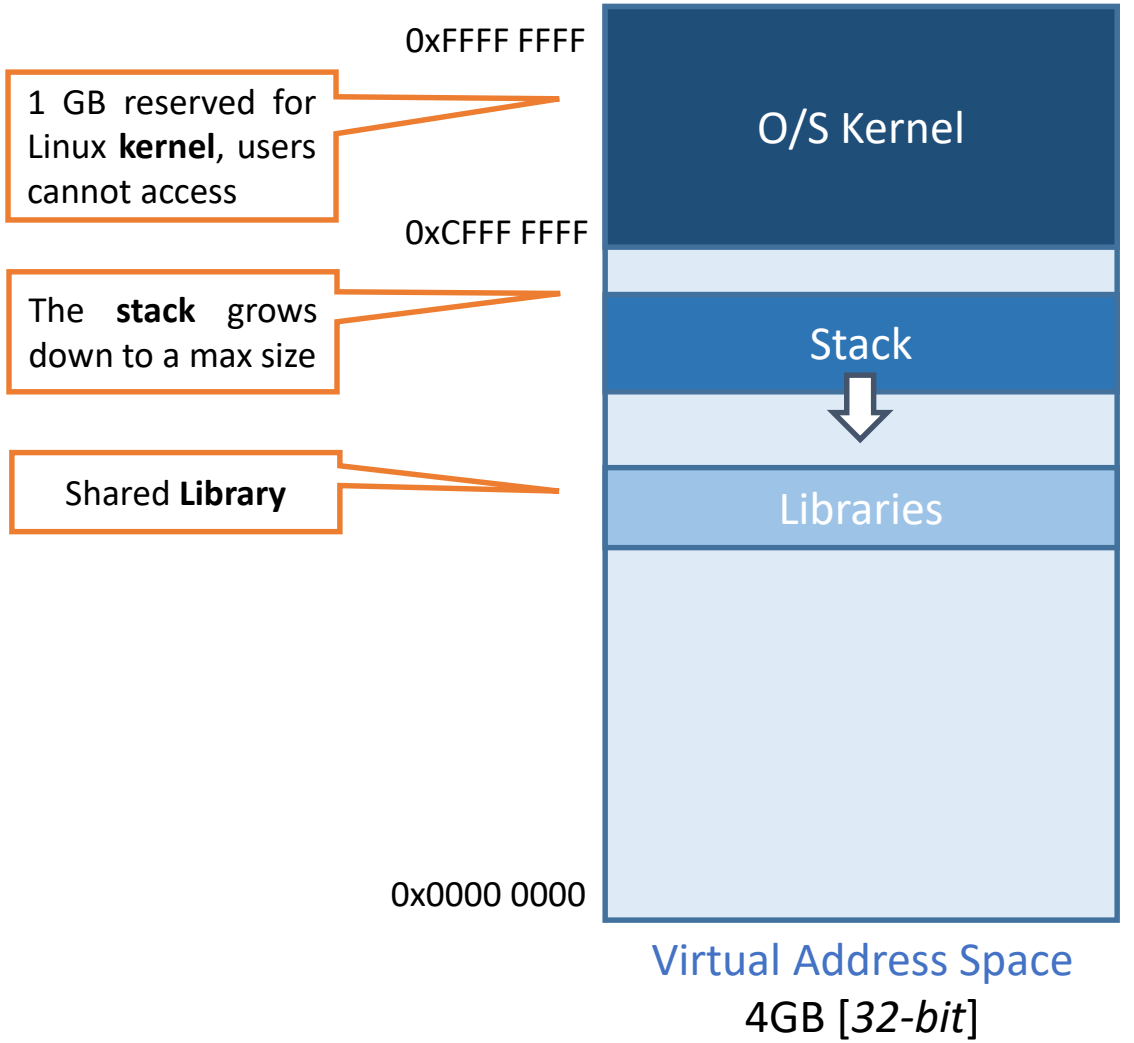

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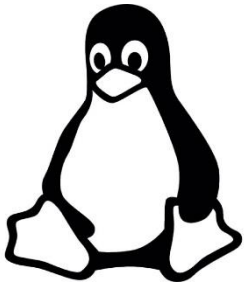

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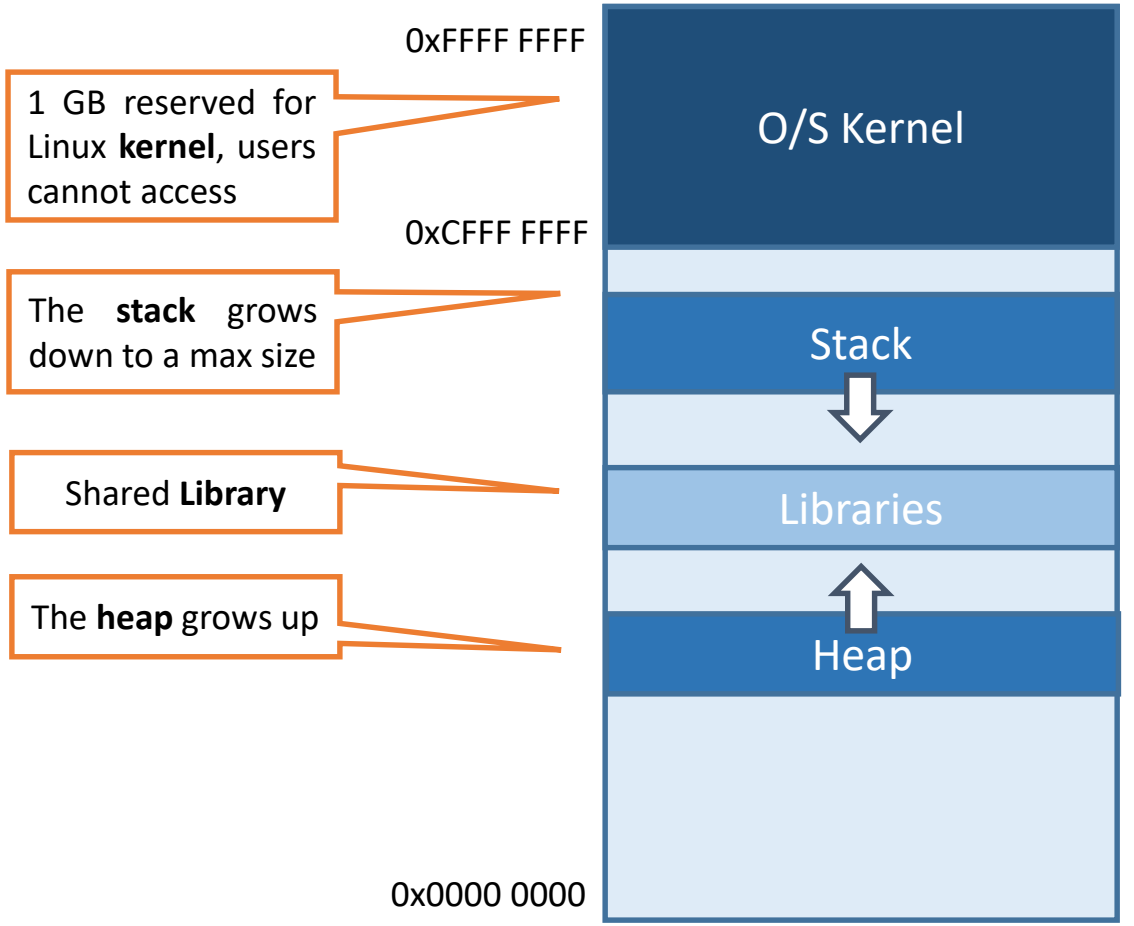

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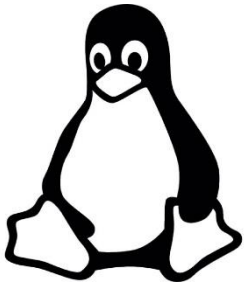

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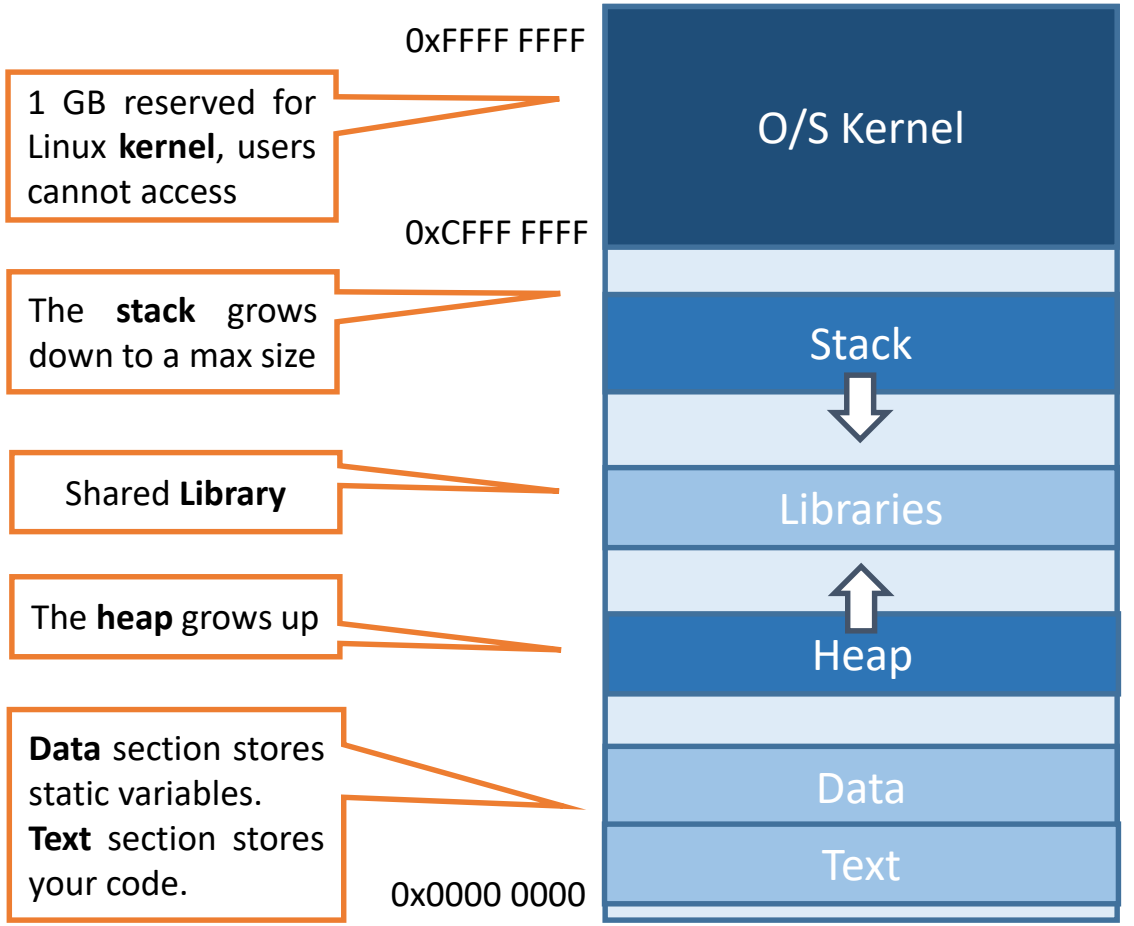

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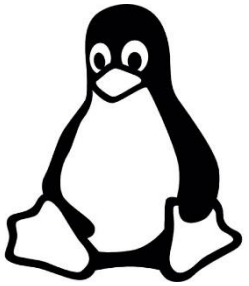

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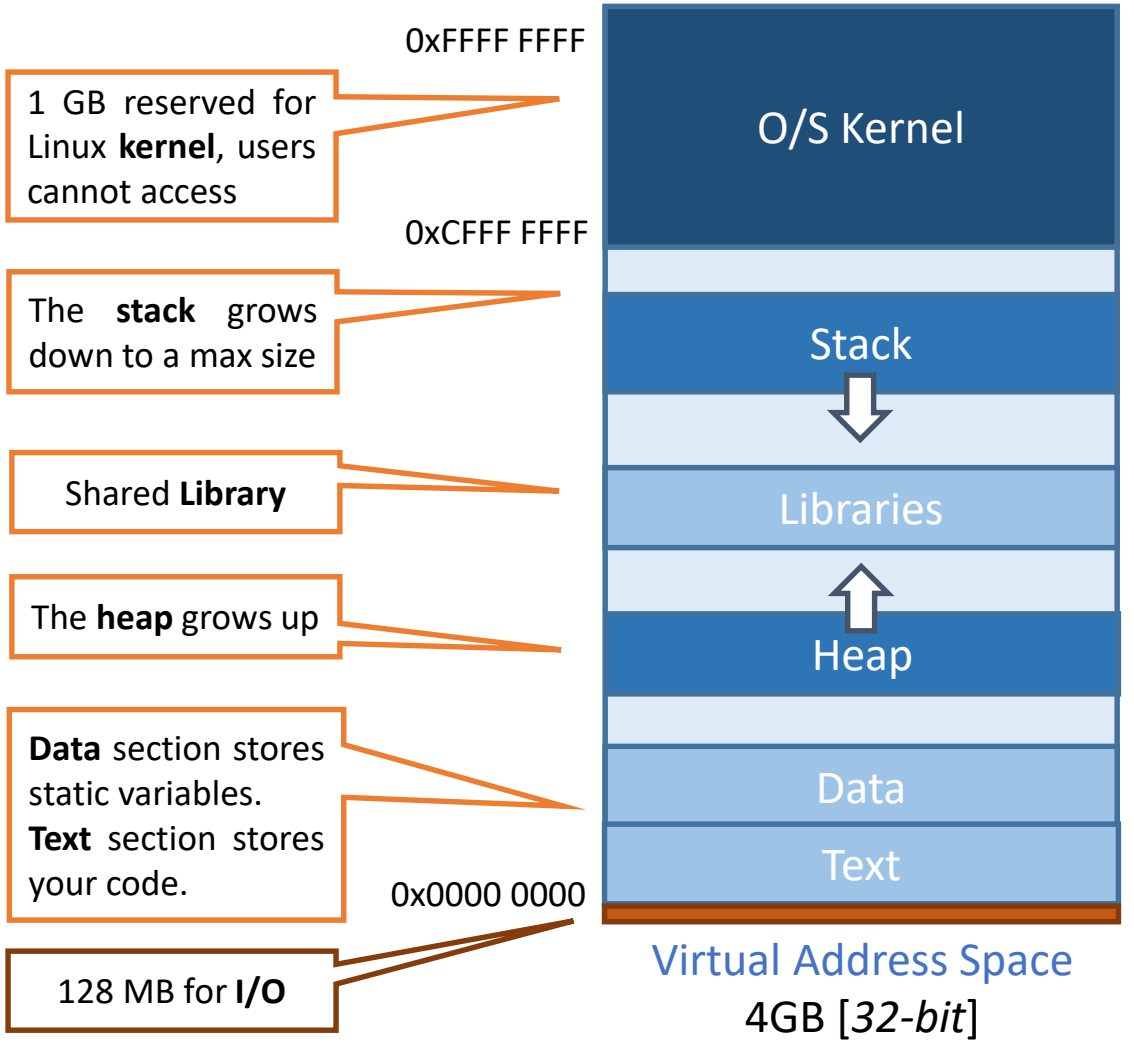

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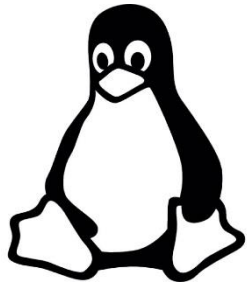

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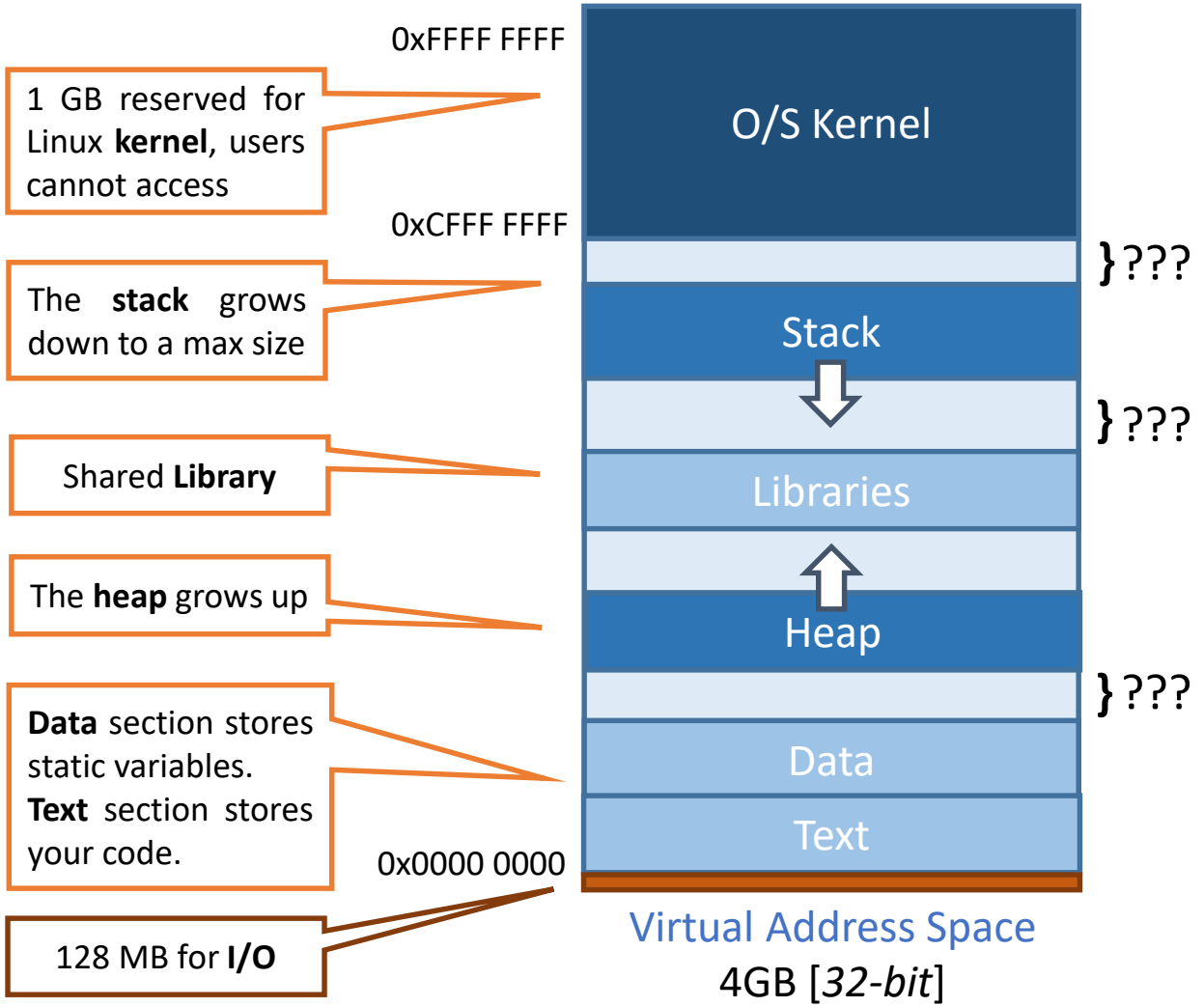
- Random offsets for security
  - Never know where code is…



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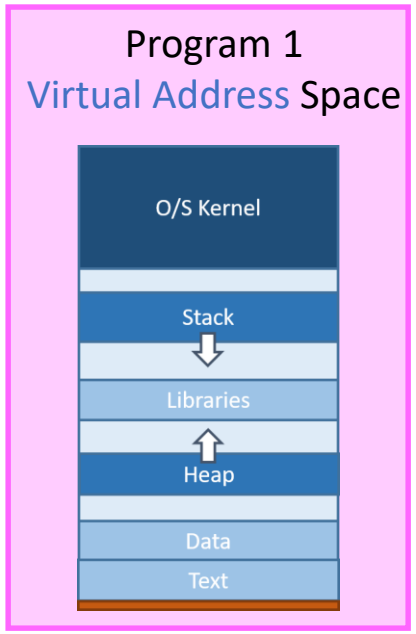
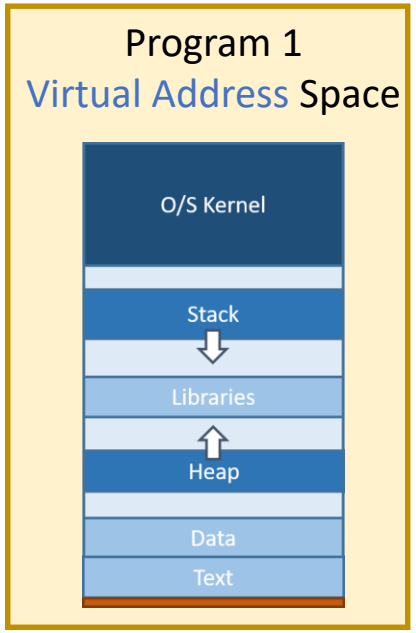
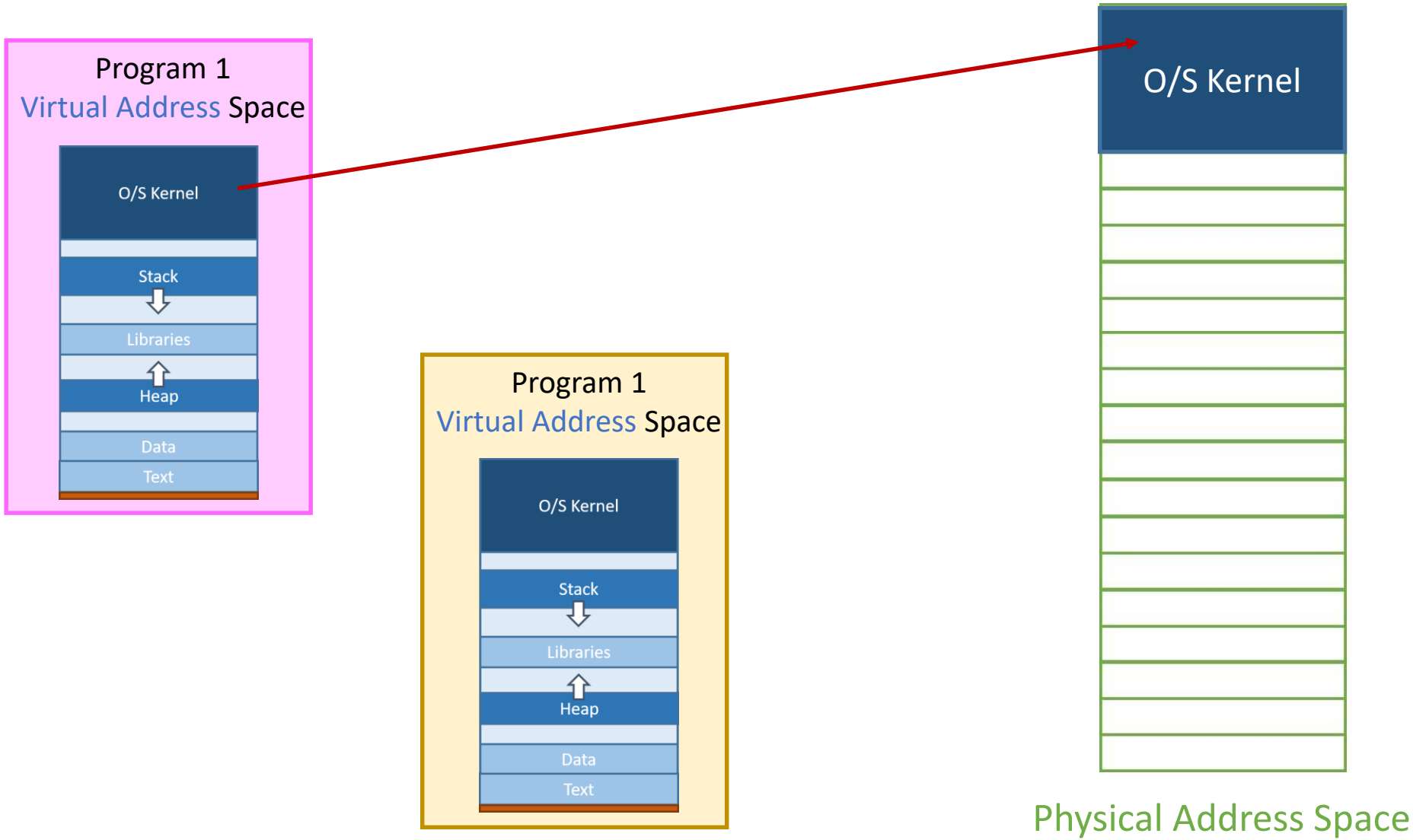


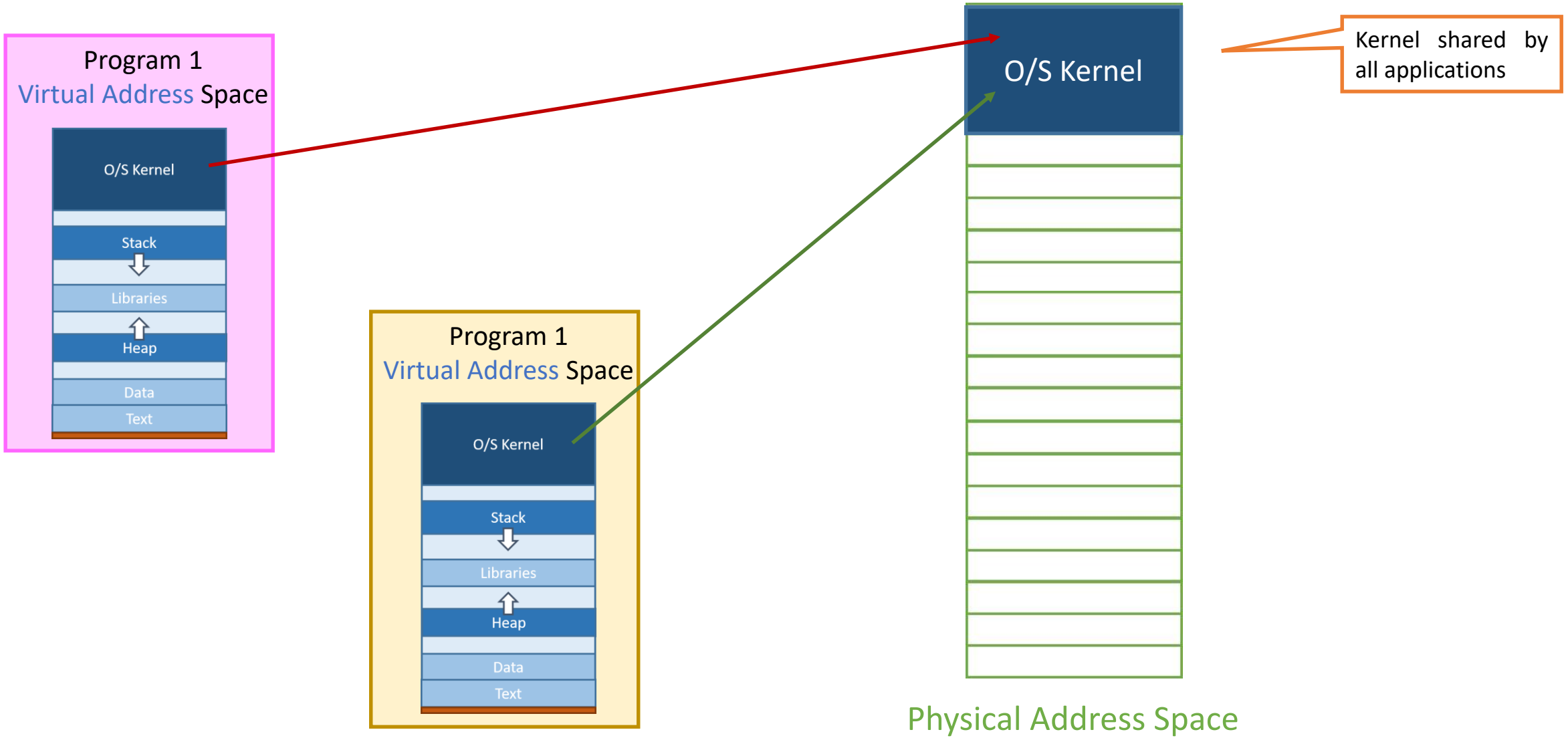


Physical Address Space

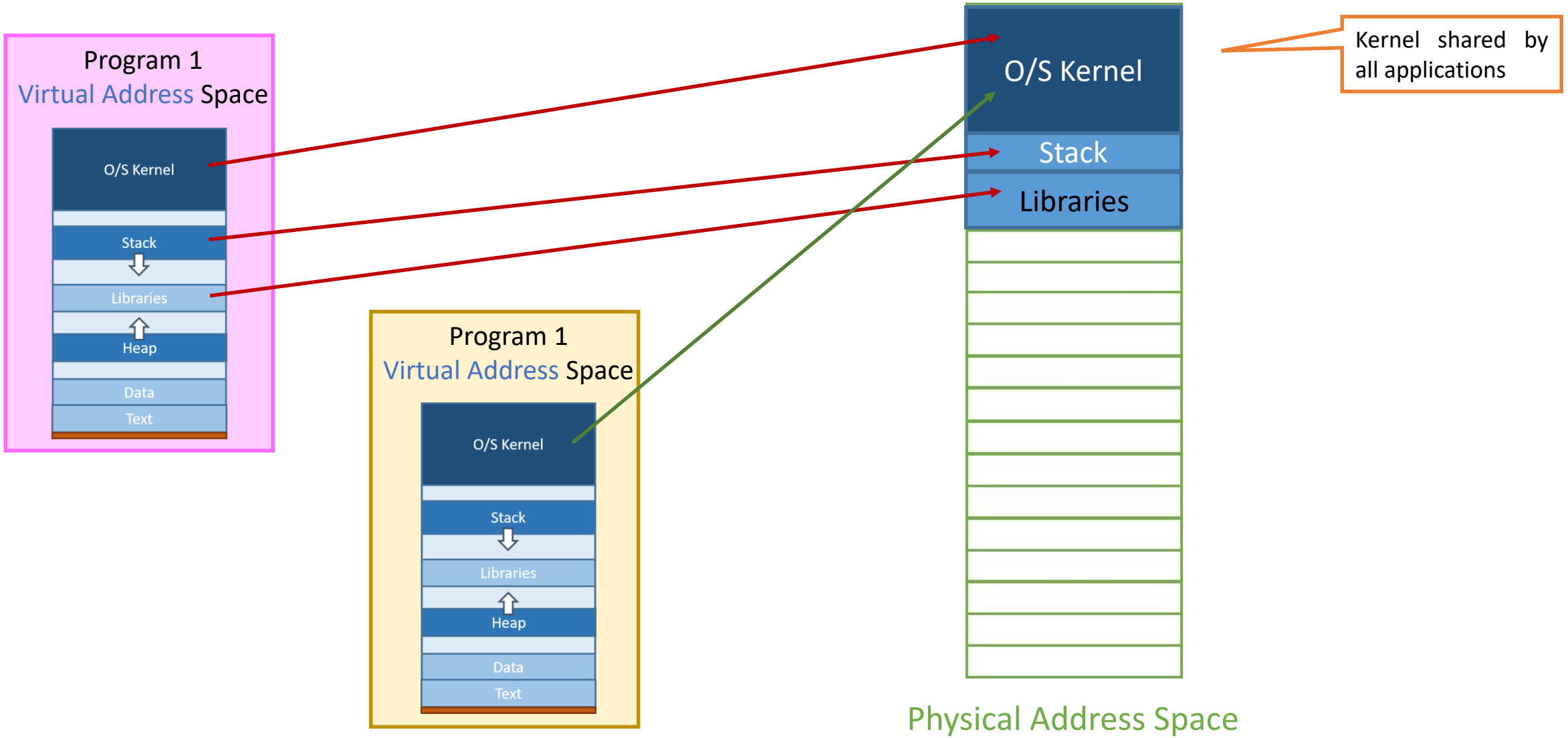
Linux Virtual Address Space



Linux Virtual Address Space



Linux Virtual Address Space



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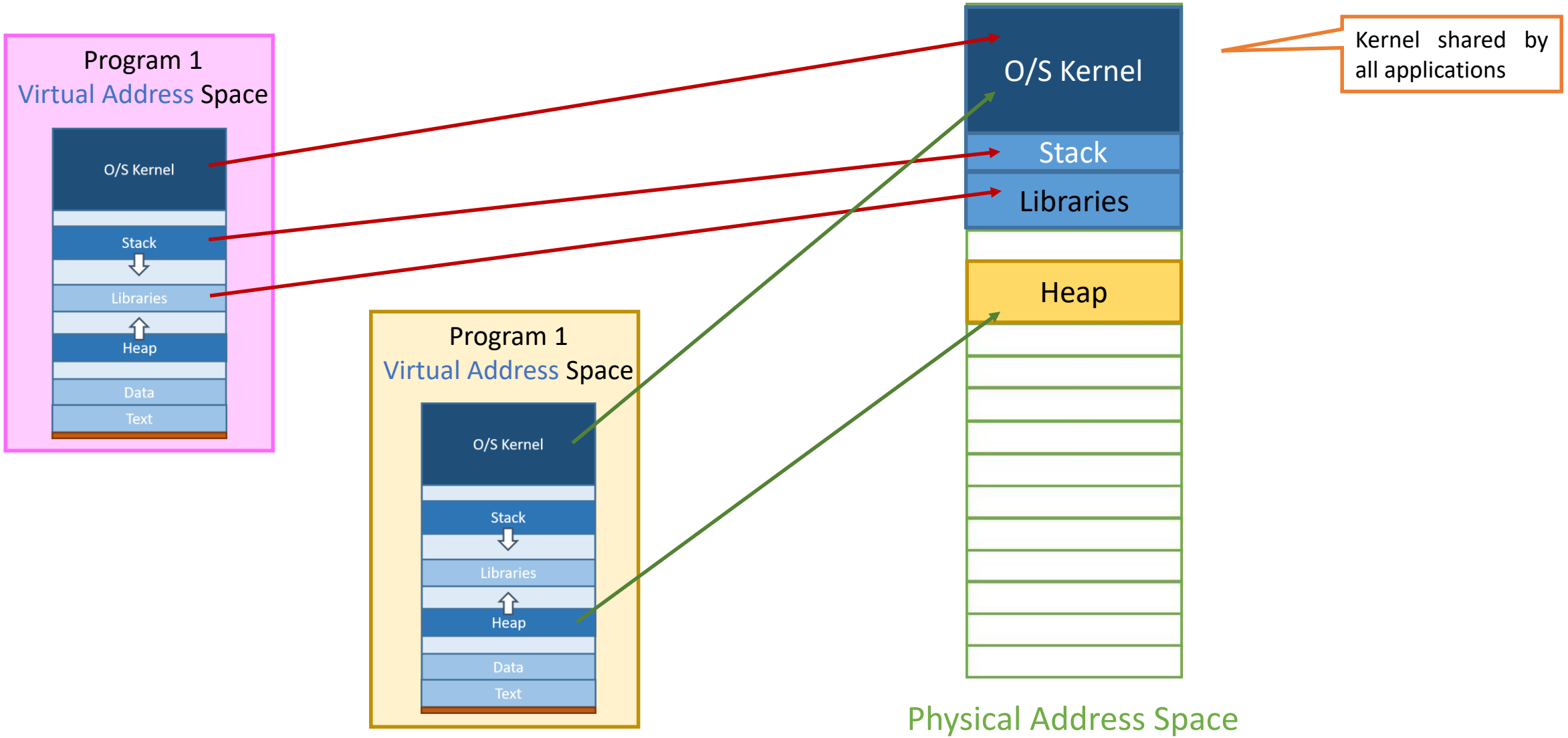

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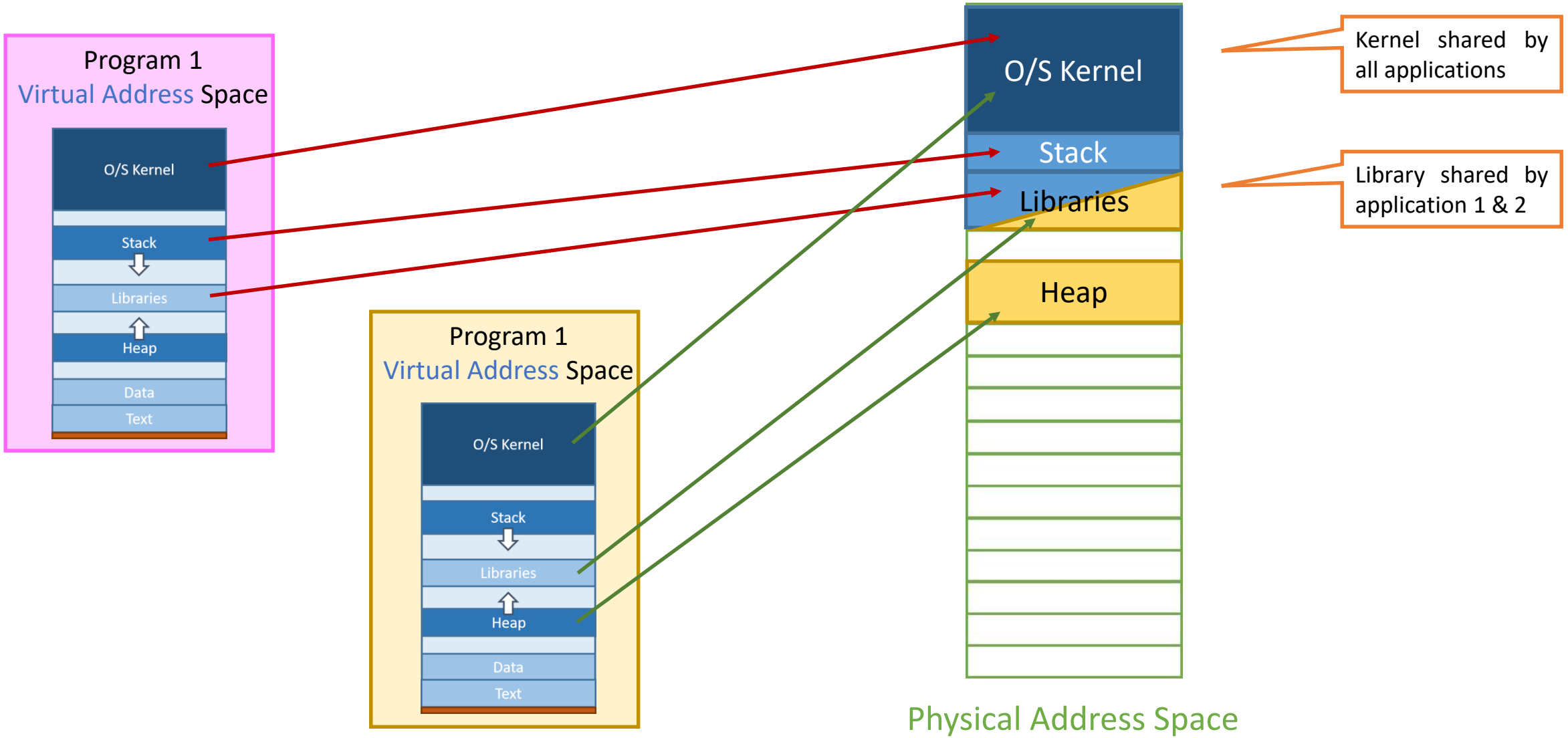
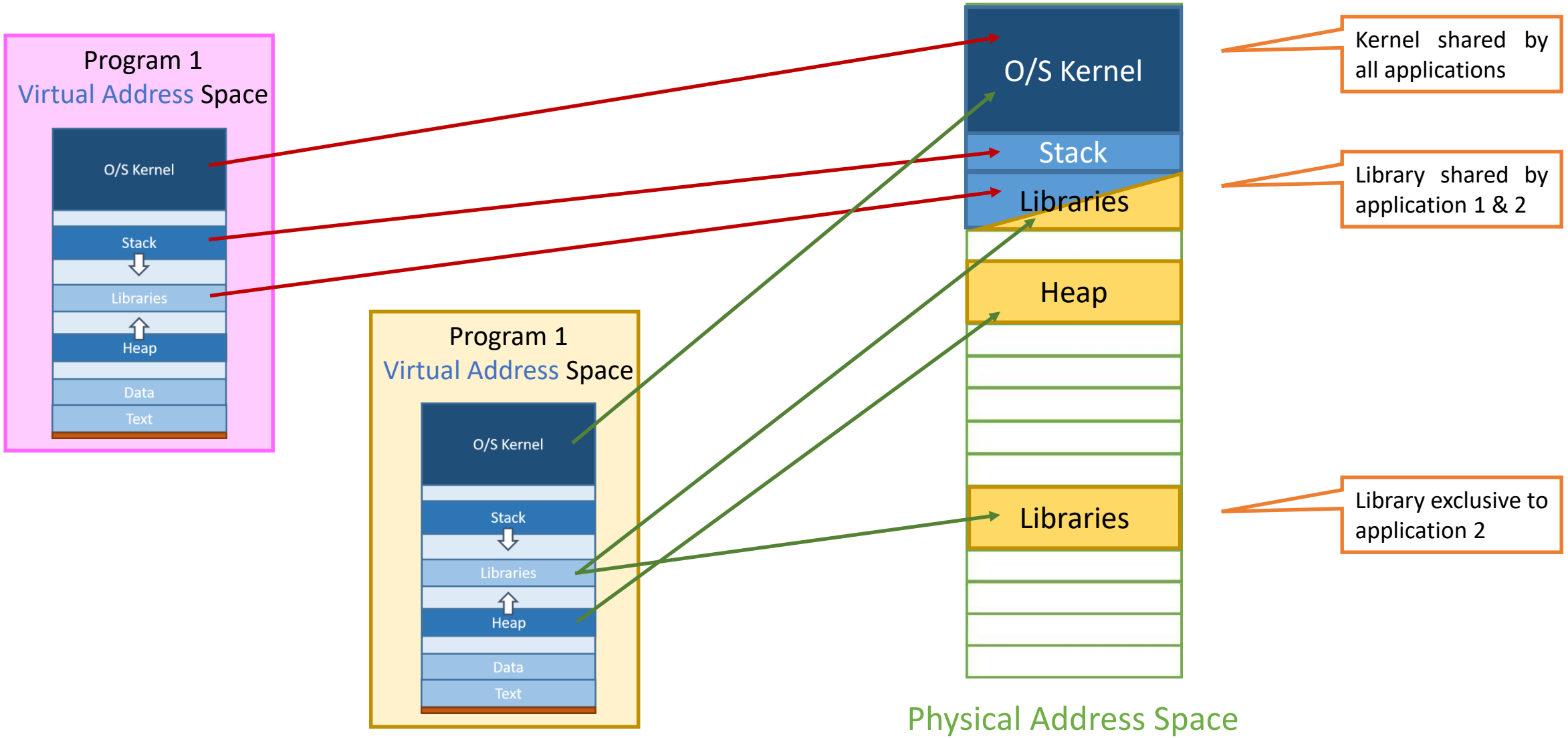


Linux Virtual Address Space



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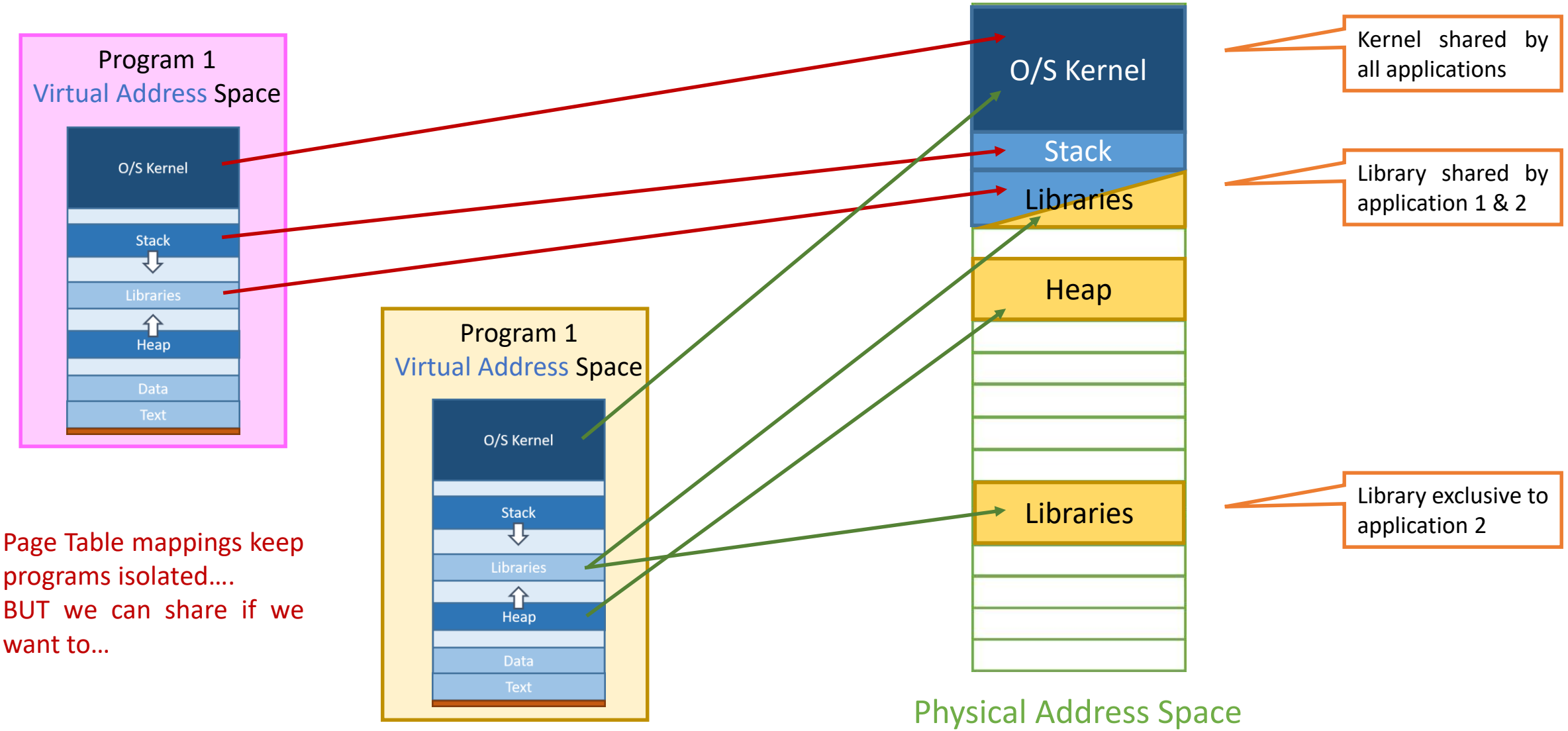
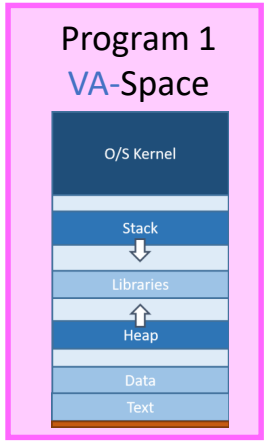
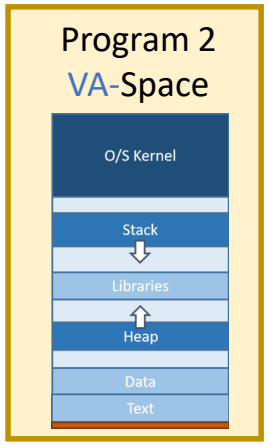
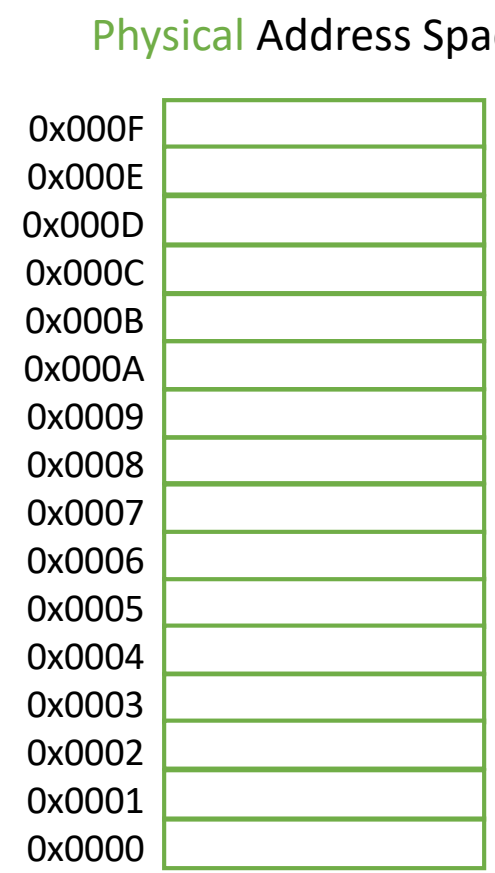


Page Table mappings keep programs isolated….
BUT we can share if we want to…

Linux Mapping Separate Address Spaces

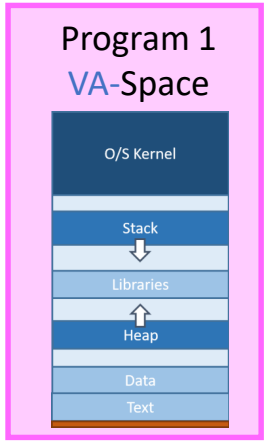






Linux Mapping Separate Address Spaces

LD $R2, 3($R0)



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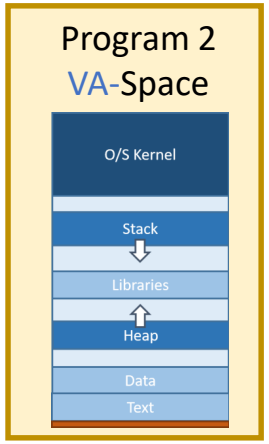

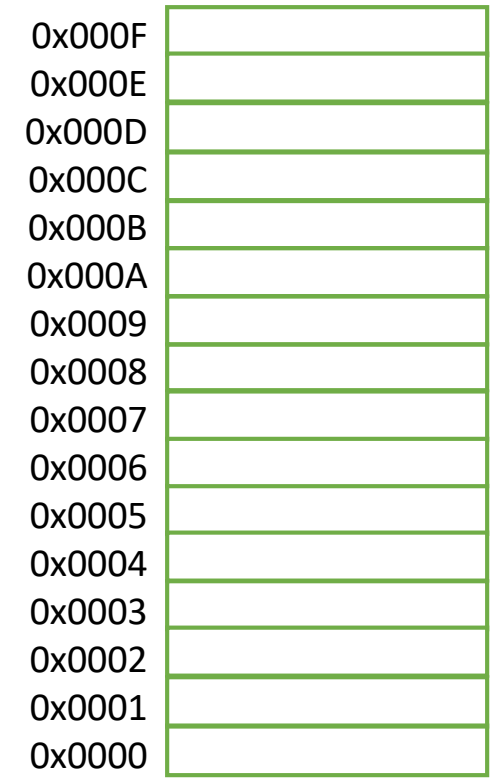

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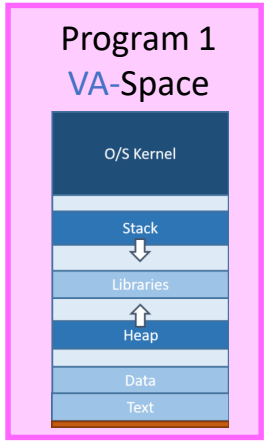

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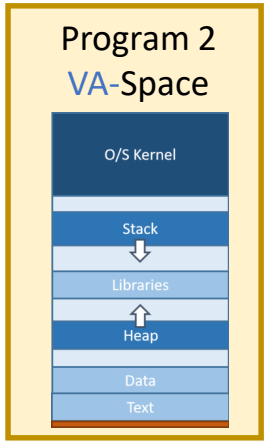
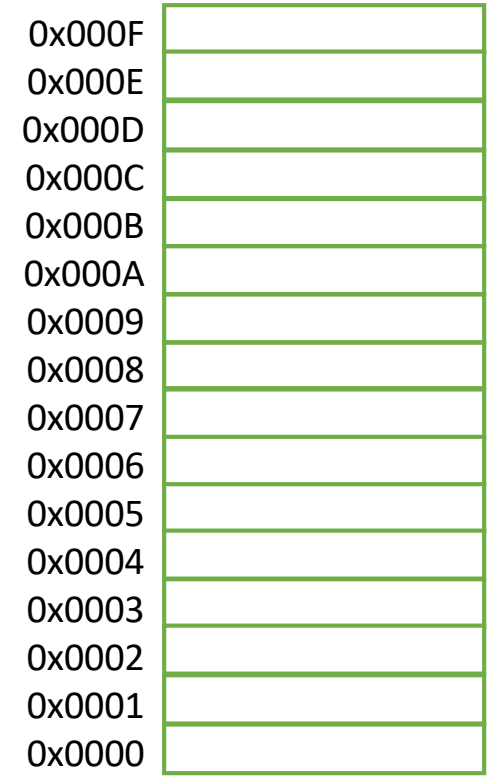


	Physical Page #
0x0 0000	0x0000
0x0 0001	0x0001
0x0 0002	0x0004
0x0 0003	0x0007
.....	.....
0xF FFFF	0x000E

Physical Address Space



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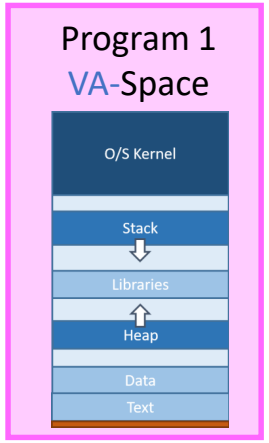

	Physical Page #
0x0 0000	0x0000
0x0 0001	0x0001
0x0 0002	0x0004
0x0 0003	0x0007
.....	.....
0xF FFFF	0x000E

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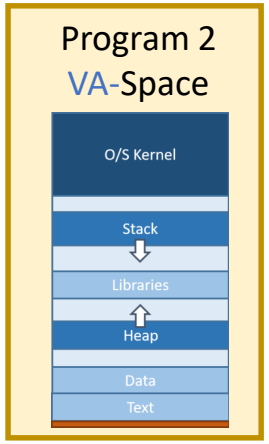
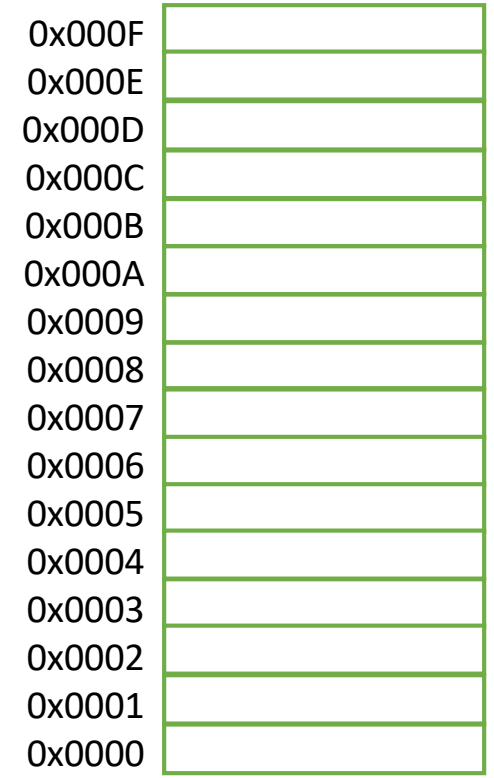


	Physical Page #
0x0 0000	0x000A
0x0 0001	0x0009
0x0 0002	0x0008
0x0 0003	0x0003
.....	.....
0xF FFFF	0x000E

Physical Address Space



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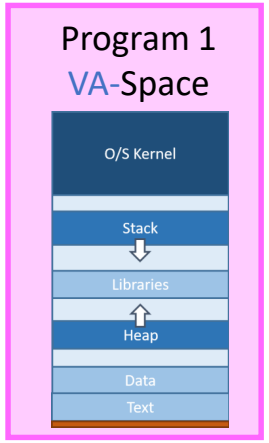

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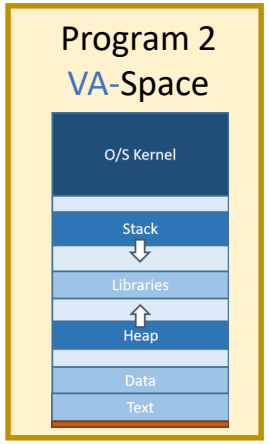


Each process gets its own Page Table

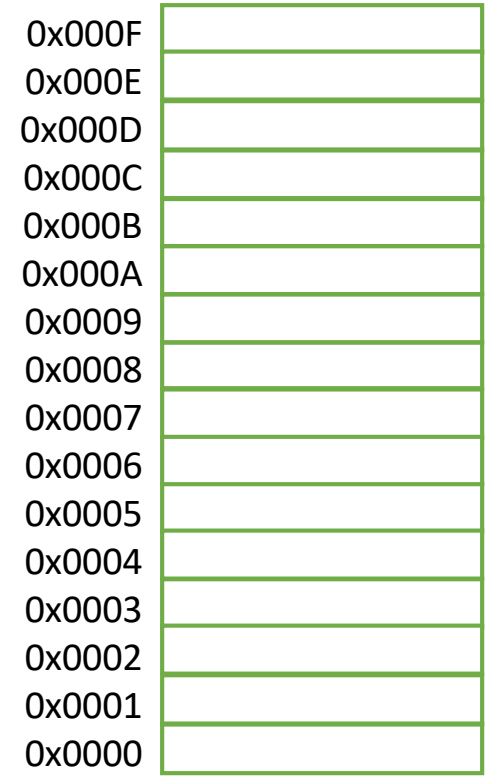
Program 1 Page Table

	Physical Page #
0x0 0000	0x0000
0x0 0001	0x0001
0x0 0002	0x0004
0x0 0003	0x0007
.....	.....
0xF FFFF	0x000E

Program 2 Page Table

	Physical Page #
0x0 0000	0x000A
0x0 0001	0x0009
0x0 0002	0x0008
0x0 0003	0x0003
.....	.....
0xF FFFF	0x000E

Physical Address Space



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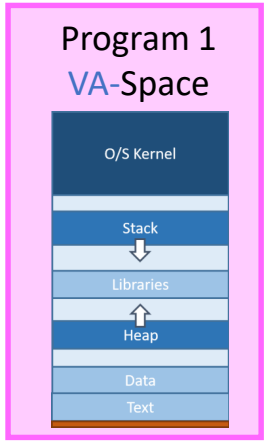

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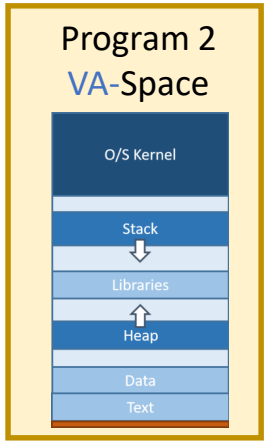


Each process gets its own Page Table

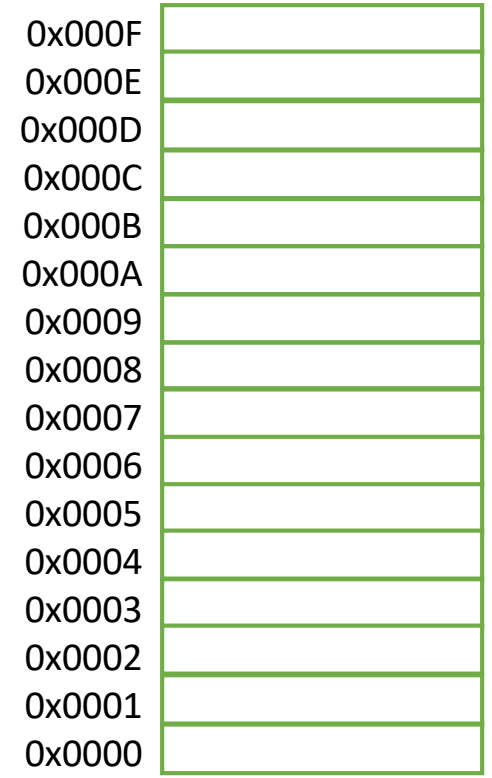
Program 1 Page Table

	Physical Page #
0x0 0000	0x0000
0x0 0001	0x0001
0x0 0002	0x0004
0x0 0003	0x0007
.....	.....
0xF FFFF	0x000E

Program 2 Page Table

	Physical Page #
0x0 0000	0x000A
0x0 0001	0x0009
0x0 0002	0x0008
0x0 0003	0x0003
.....	.....
0xF FFFF	0x000E

Physical Address Space



Linux Mapping Separate Address Spaces

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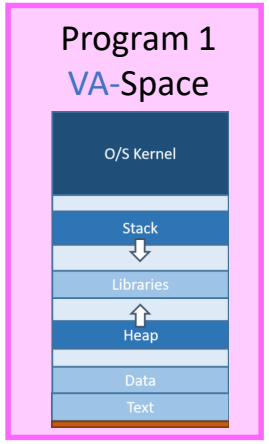
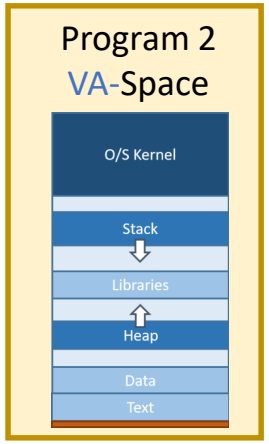


VA=3

Program 1 Page Table

	Physical Page #
0x0 0000	0x0000
0x0 0001	0x0001
0x0 0002	0x0004
0x0 0003	0x0007
.....	.....
0xF FFFF	0x000E

LD $R2, 3($R0)



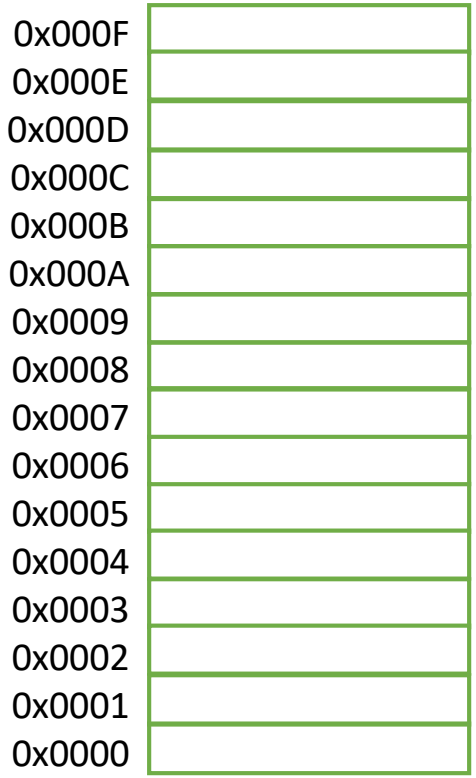
VA=3

Program 2 Page Table

	Physical Page #
0x0 0000	0x000A
0x0 0001	0x0009
0x0 0002	0x0008
0x0 0003	0x0003
.....	.....
0xF FFFF	0x000E

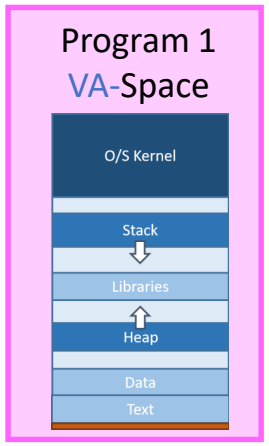
Each process gets its own Page Table

Physical Address Space



Linux Mapping Separate Address Spaces

LD $R2, 3($R0)



VA=3

Program 1 Page Table

	Physical Page #
0x0 0000	0x0000
0x0 0001	0x0001
0x0 0002	0x0004
0x0 0003	0x0007
.....	.....
0xF FFFF	0x000E

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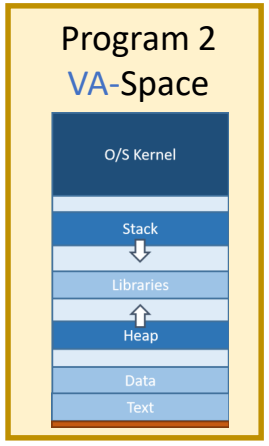


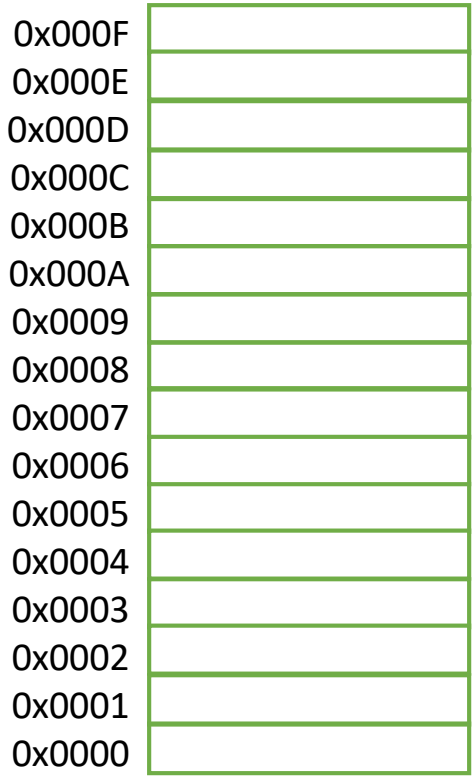
VA=3

Program 2 Page Table

	Physical Page #
0x0 0000	0x000A
0x0 0001	0x0009
0x0 0002	0x0008
0x0 0003	0x0003
.....	.....
0xF FFFF	0x000E

Each process gets its own Page Table

Physical Address Space



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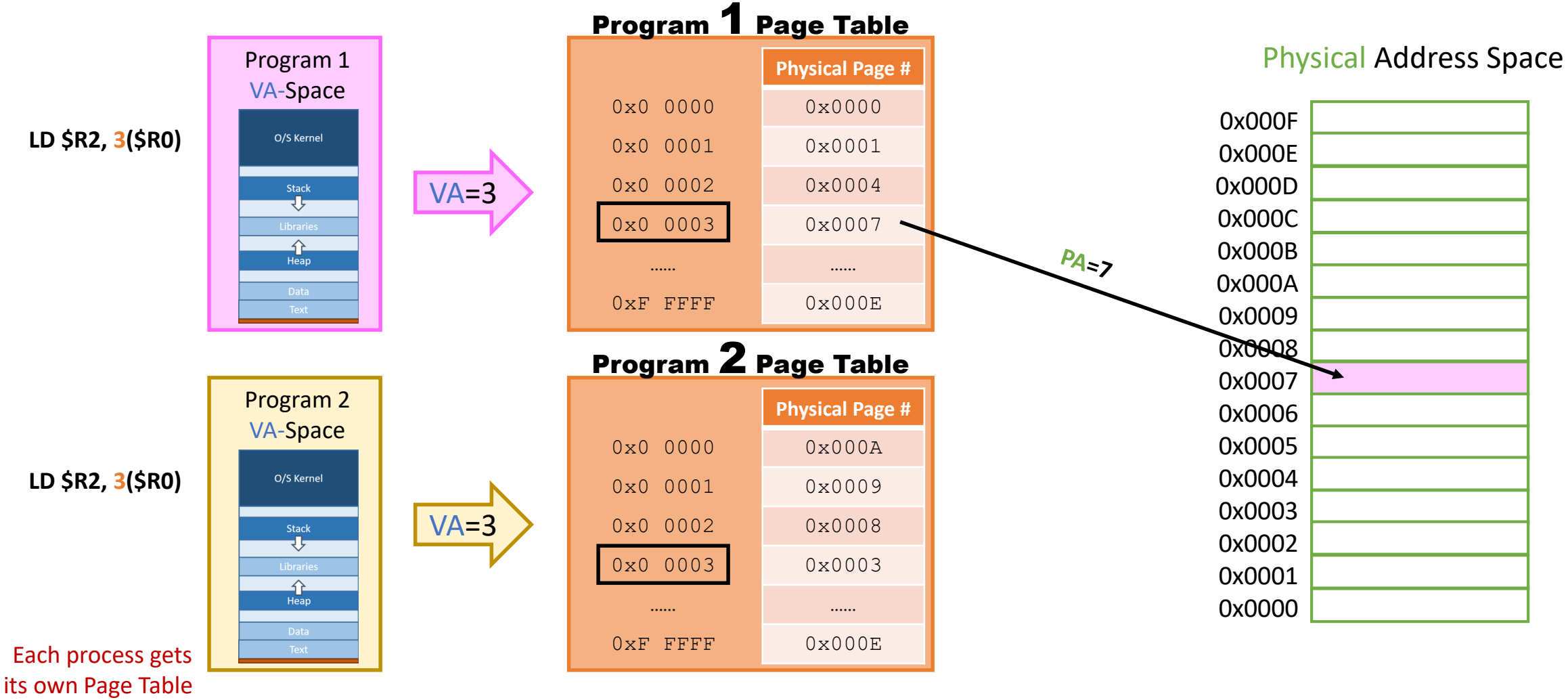

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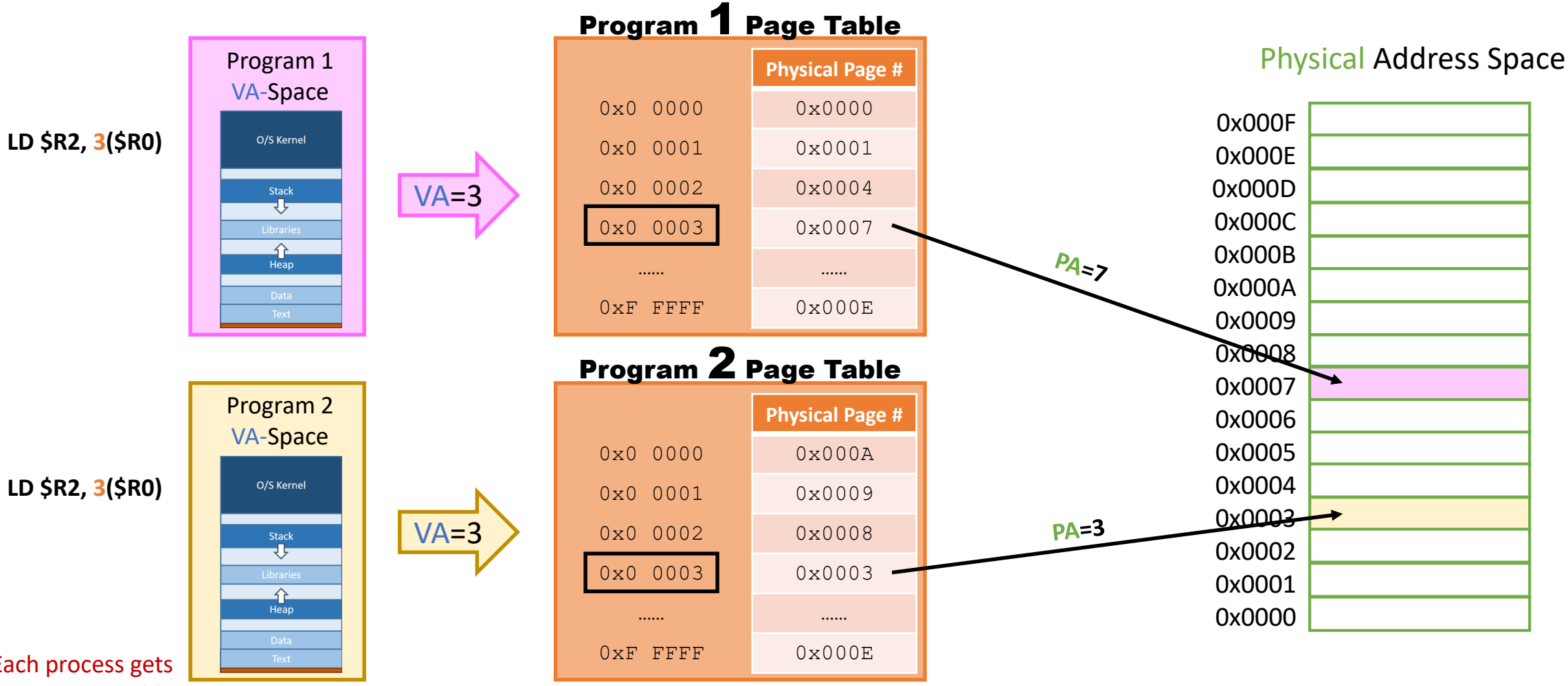

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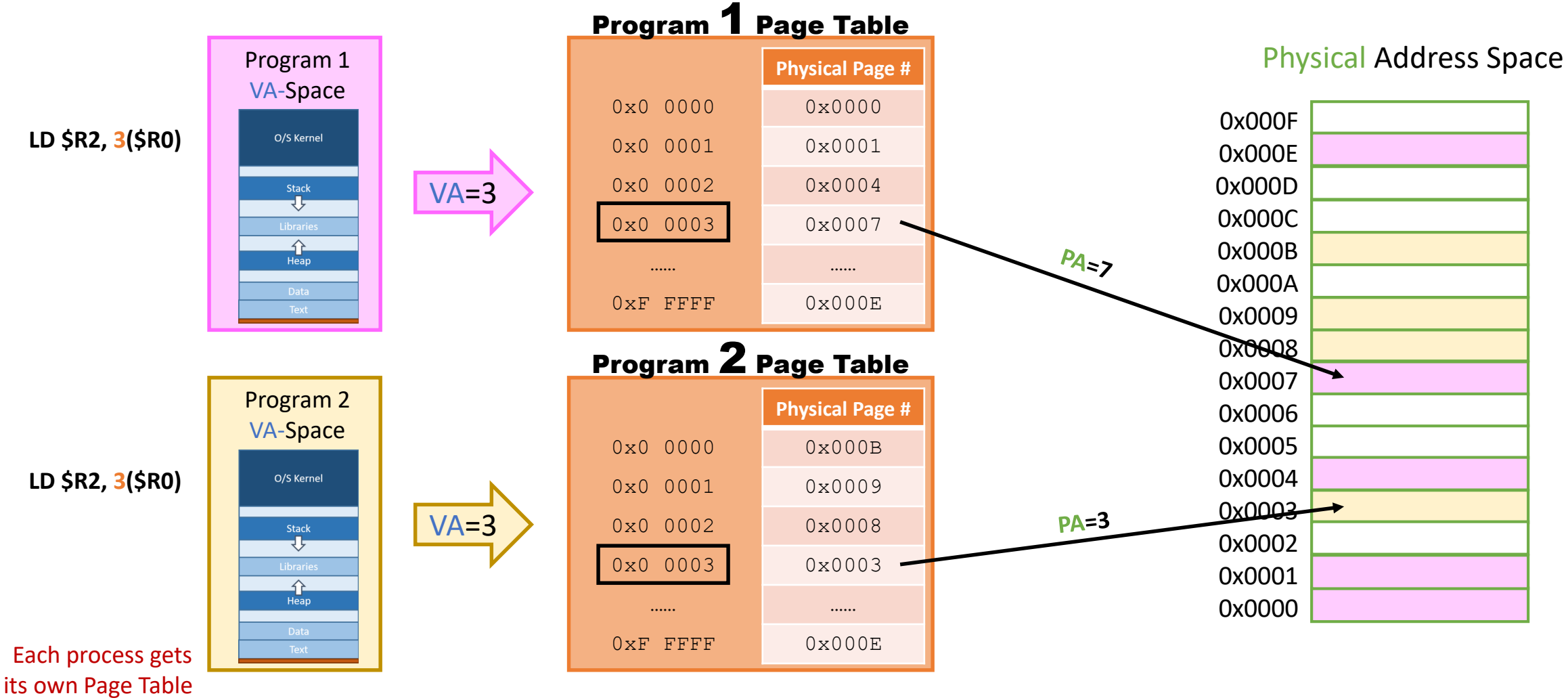

Quiz: Memory Protection

Q: Which of the following Page Table Entries can cause data corruption?

- **Program 1** 0x00003, **Program 2** 0x00003
- **Program 1** 0x00002, **Program 2** 0x00000
- **Program 1** 0xFFFFF, **Program 2** 0xFFFFF
- None of these

Program 1 Page Table

	Physical Page #
0x0 0000	0x0000
0x0 0001	0x0001
0x0 0002	0x0004
0x0 0003	0x0007
.....	.....
0xF FFFF	0x000E

Program 2 Page Table

	Physical Page #
0x0 0000	0x0004
0x0 0001	0x0006
0x0 0002	0x000C
0x0 0003	0x000D
.....	.....
0xF FFFF	0x00FF

Quiz: Memory Protection

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- **Program 1** 0xFFFFF, **Program 2** 0xFFFFF
- None of these

A: Program 1 0x00002, Program 2 0x00000.

These Virtual Addresses point to the same Physical Address. This can cause data corruption if care is not taken. These programs can safely share data, however.

Program 1 Page Table

	Physical Page #
0x0 0000	0x0000
0x0 0001	0x0001
0x0 0002	0x0004
0x0 0003	0x0007
.....	.....
0xF FFFF	0x000E

Program 2 Page Table

	Physical Page #
0x0 0000	0x0004
0x0 0001	0x0006
0x0 0002	0x000C
0x0 0003	0x000D
.....	.....
0xF FFFF	0x00FF

Quincy Flint

Making VM Fast

Quiz: Memory Access under VM

Q: Which of the following occur for *each* memory access under Virtual Memory? Select all that apply…

I. Translate the address
II. Load data from disk
III. Update the cache
IV. Reference the Page Table
V. Update the Page Table
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A:

I. Translate the address
IV. Reference the Page Table
VI. Access data in RAM

The others can occur, but do not happen on every memory access.

Making Virtual Memory Fast

Quincy Flint

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- Virtual Memory solves our 3 memory problems
  - “unlimited” memory, data fragmentation, data corruption

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- We need to make the Page Table look-up very fast
  - If not, VM is not tenable…
  - Cannot do this in software (this adds 10’s of instructions)
  - Must do this in hardware… use another layer of **cache**

Making Virtual Memory Fast: TLB

- Translation Lookaside Buffer (TLB): special page table cache to make VM fast

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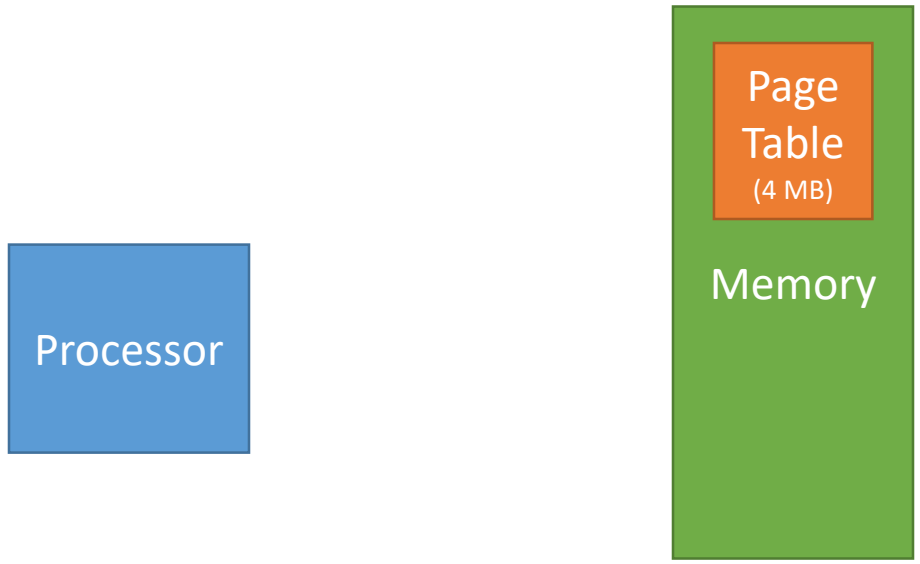

Making Virtual Memory Fast: TLB

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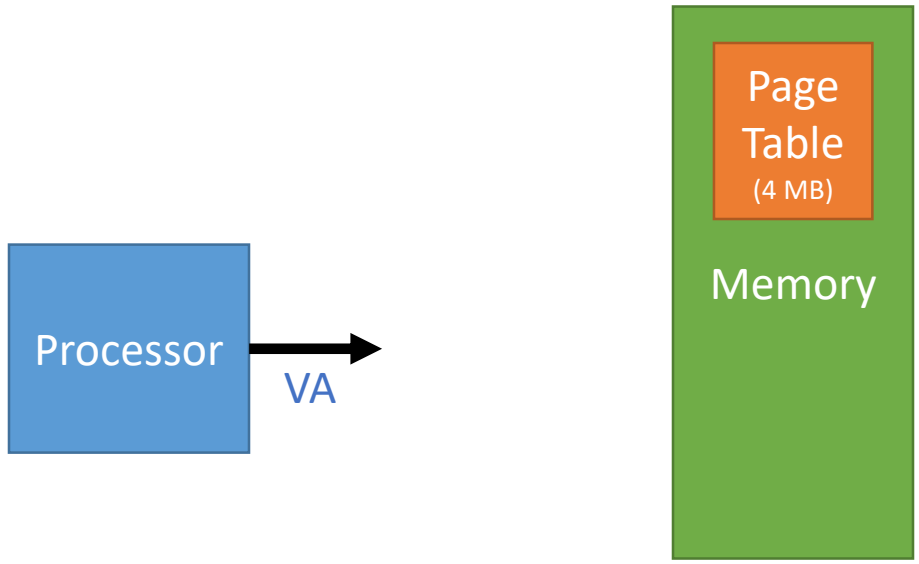

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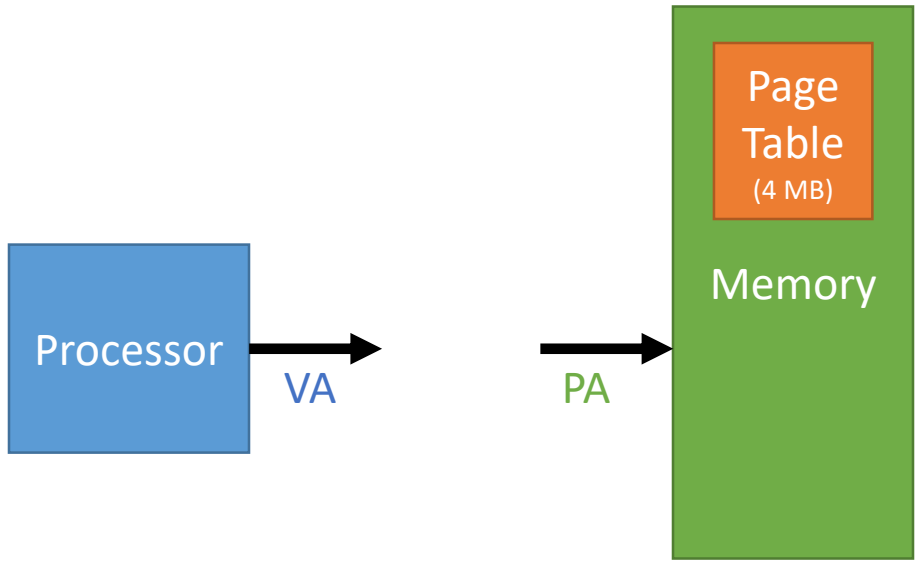

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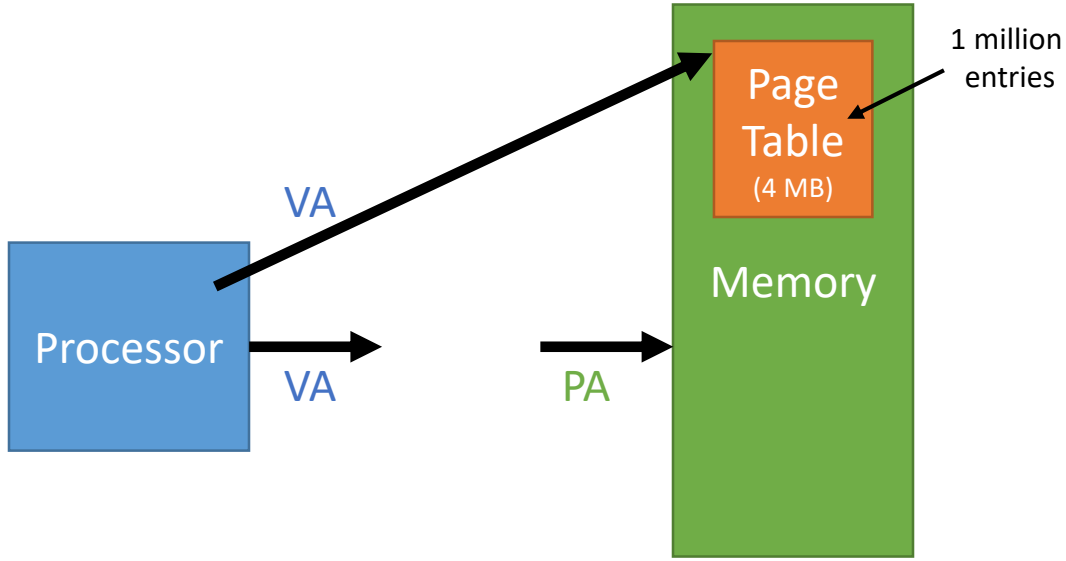

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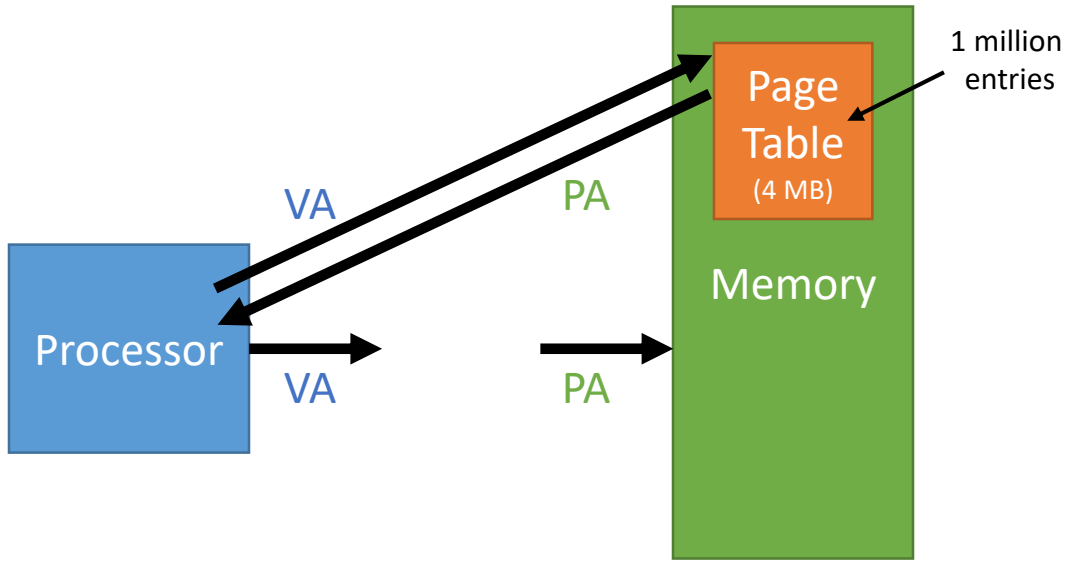

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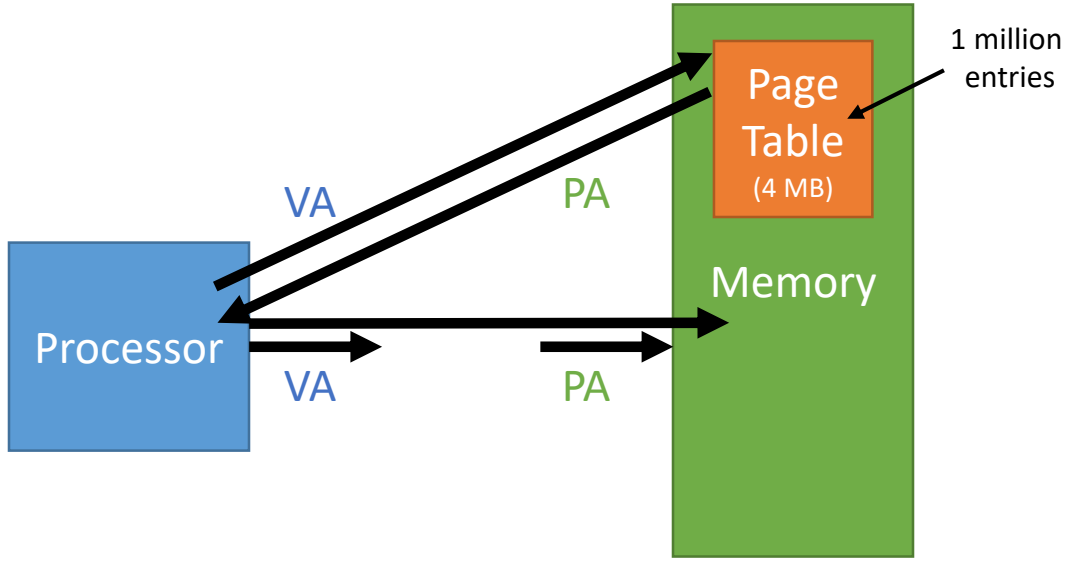

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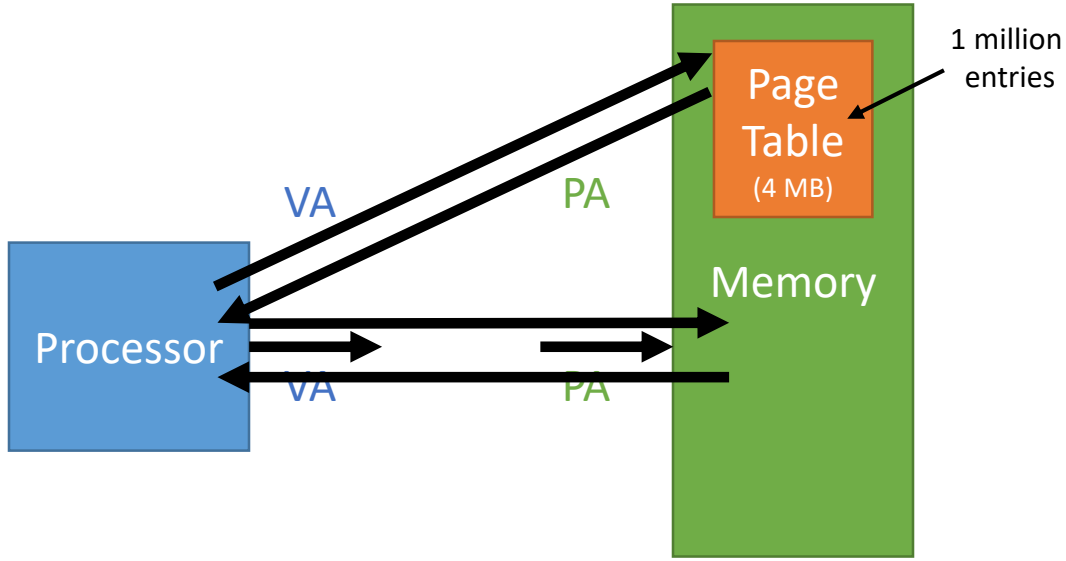

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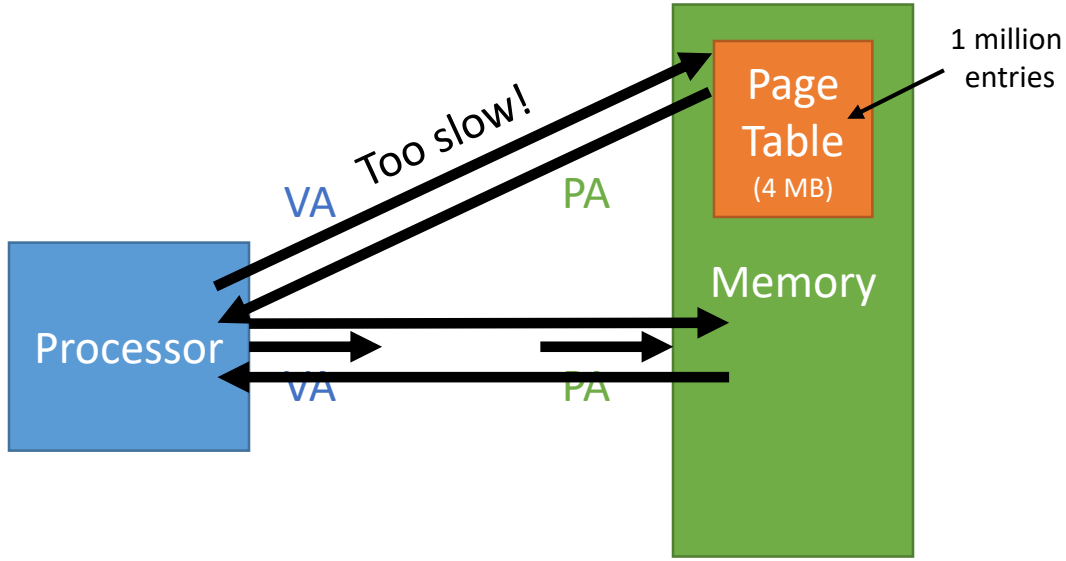

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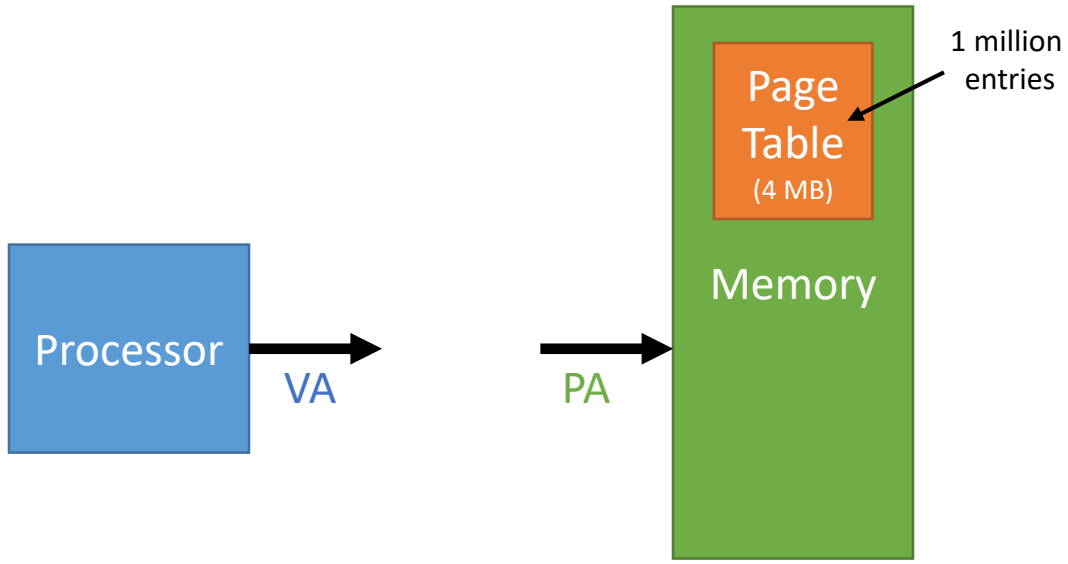

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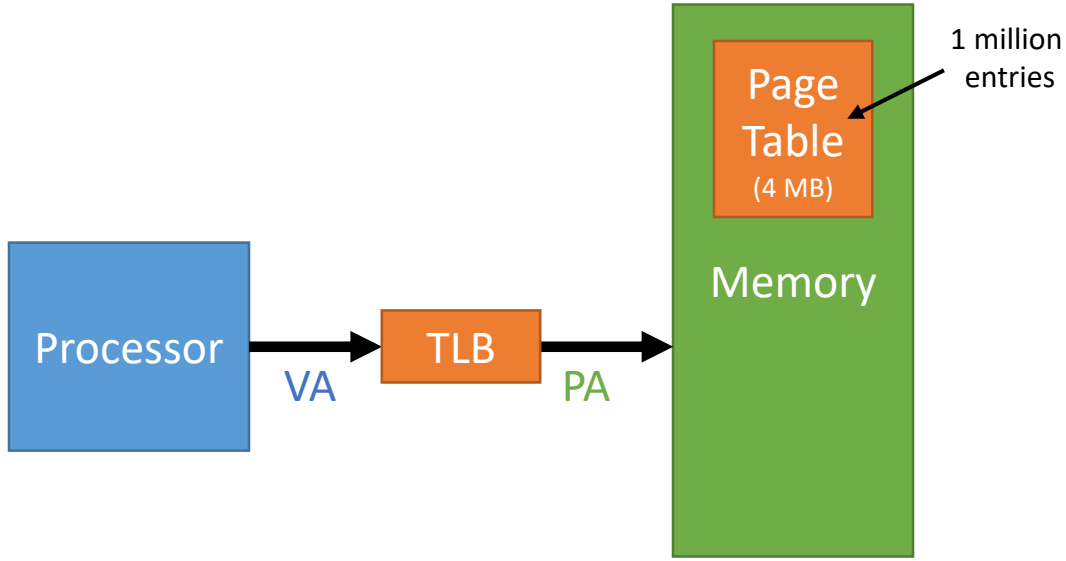

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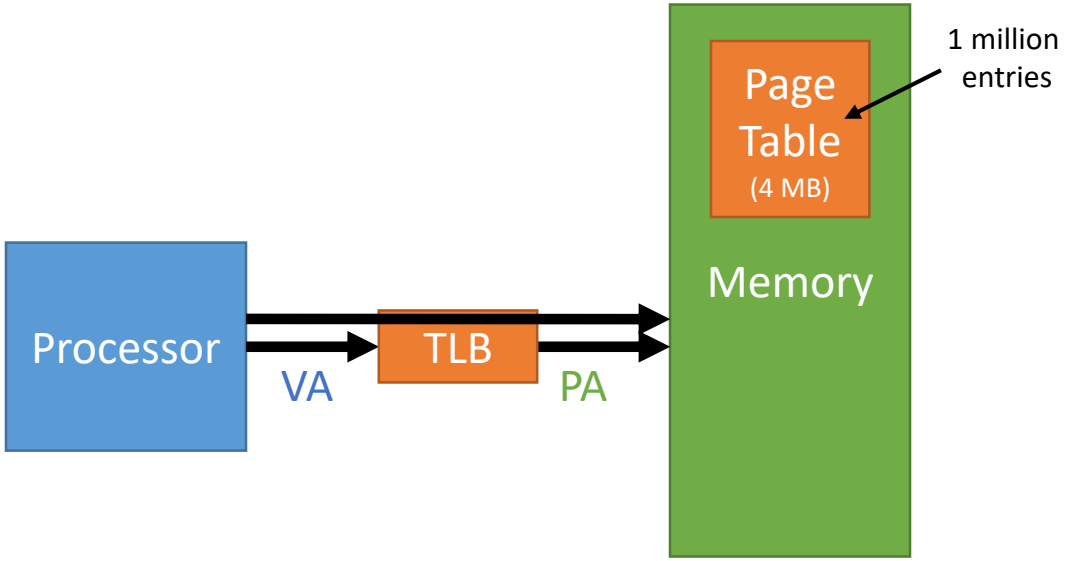

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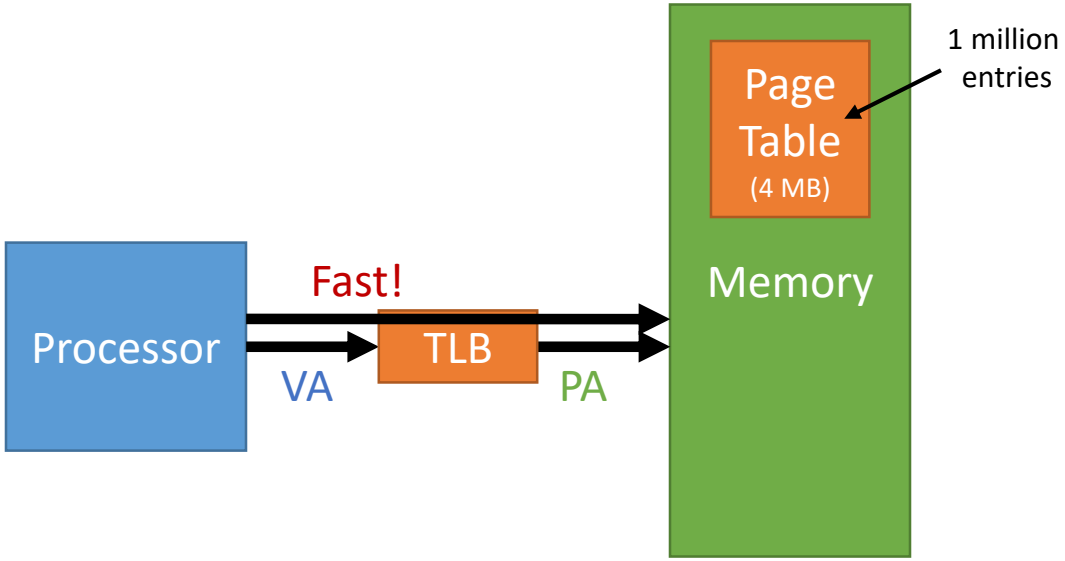

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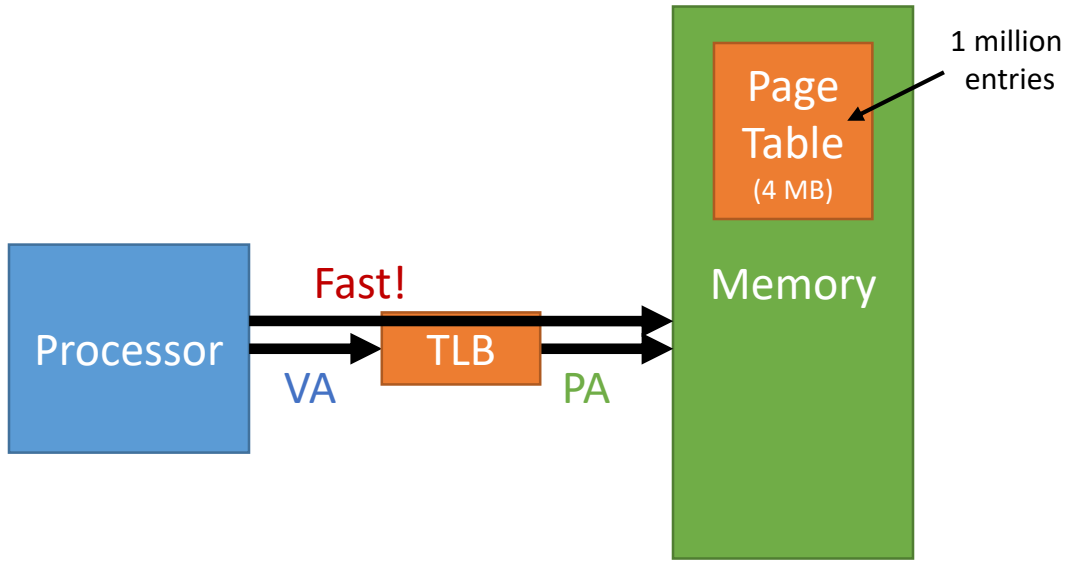

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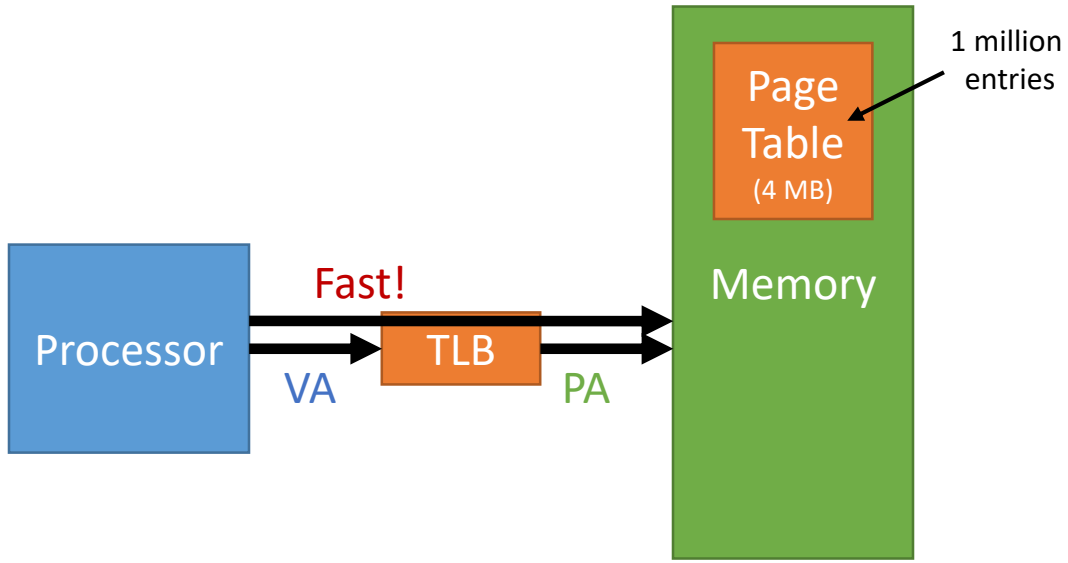

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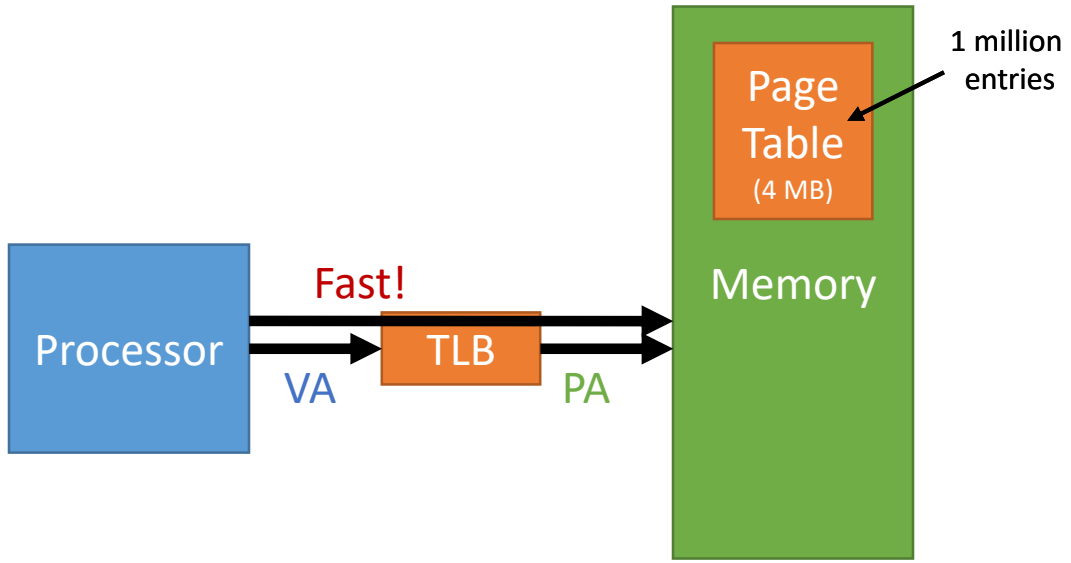

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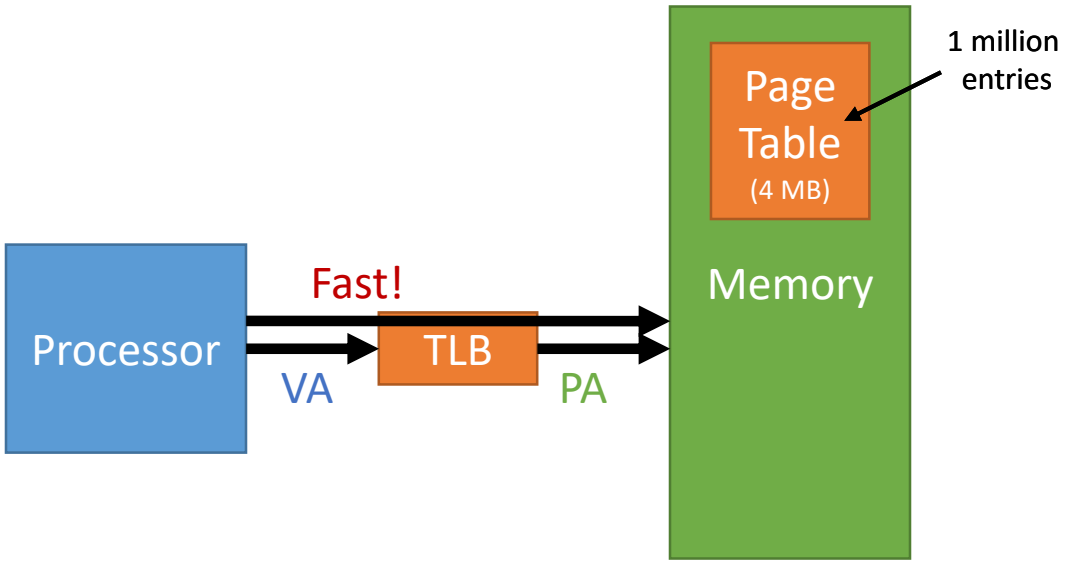

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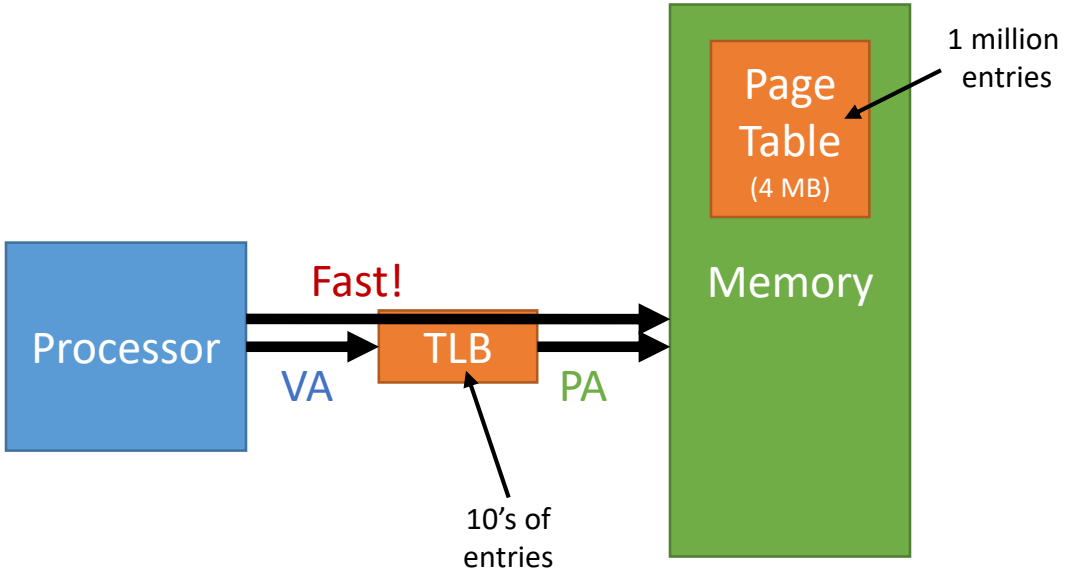

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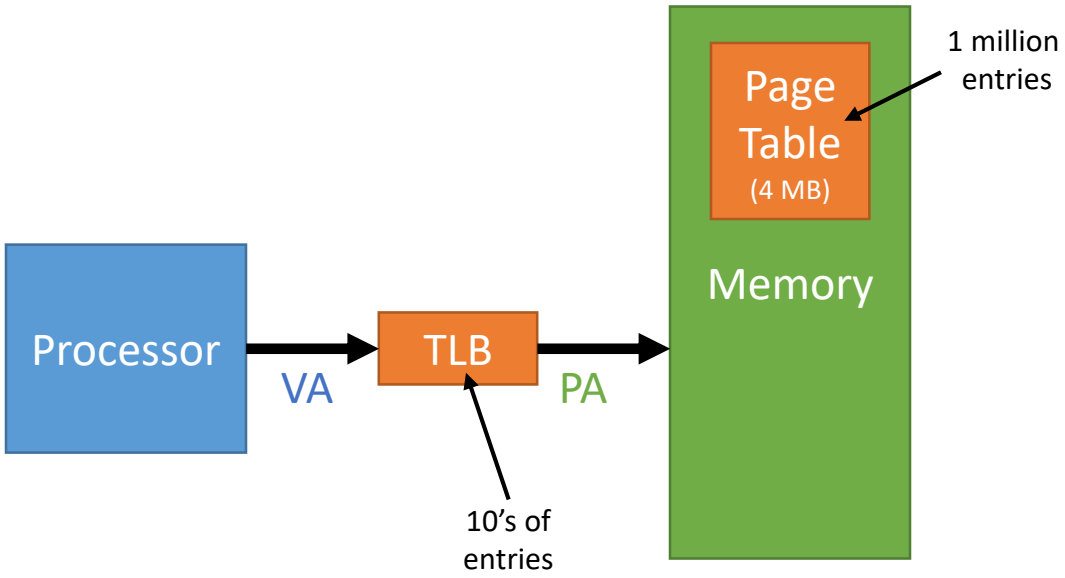
Page Table has 1 million entry, TLB only has 10's of entries??

Each Page maps 4k addresses, exploit principal of locality!



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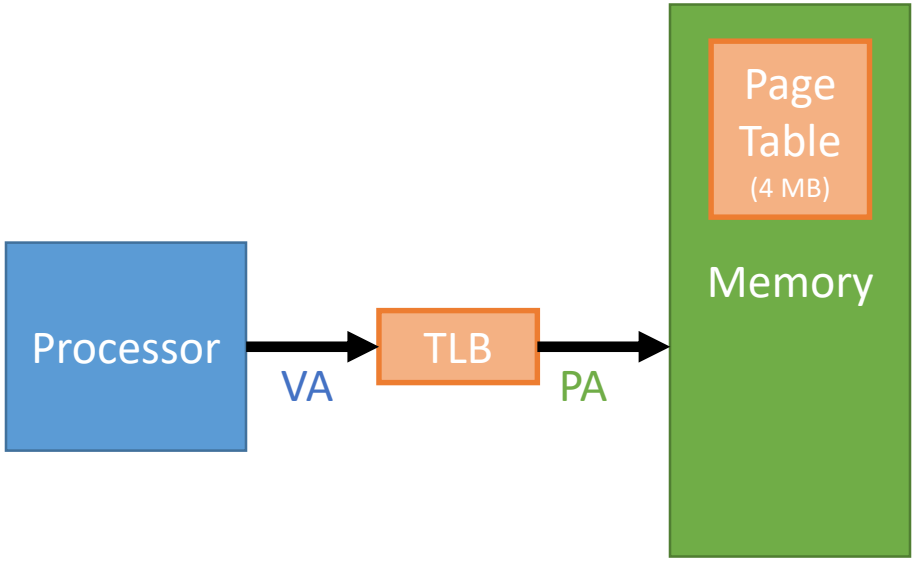

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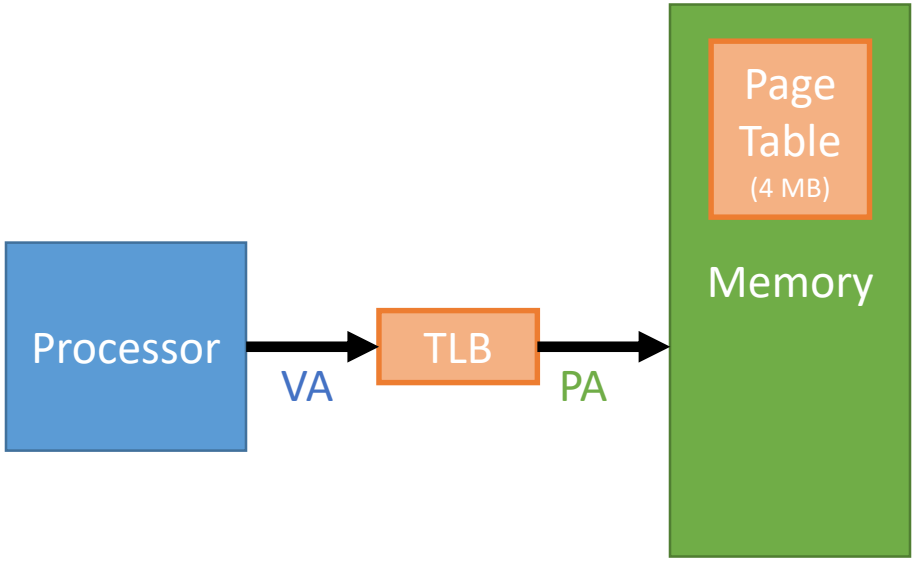

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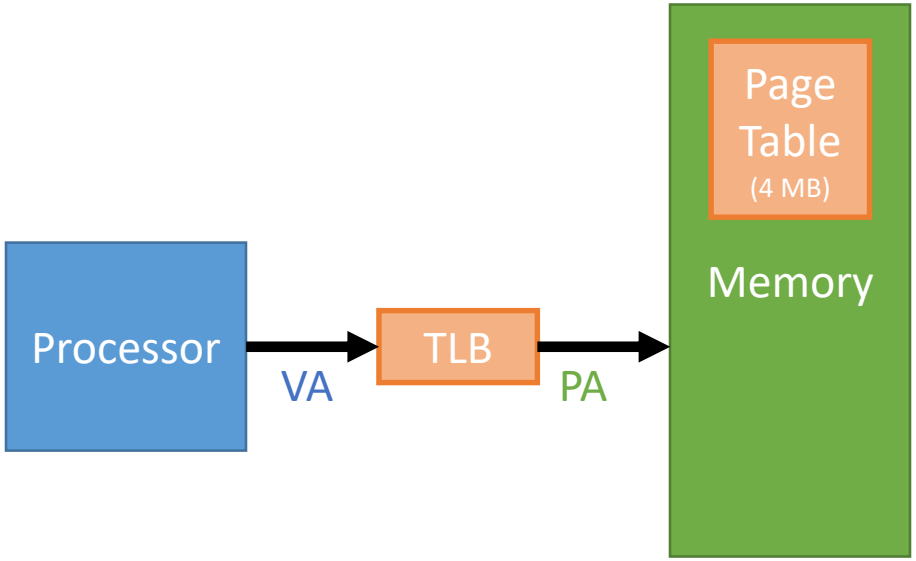

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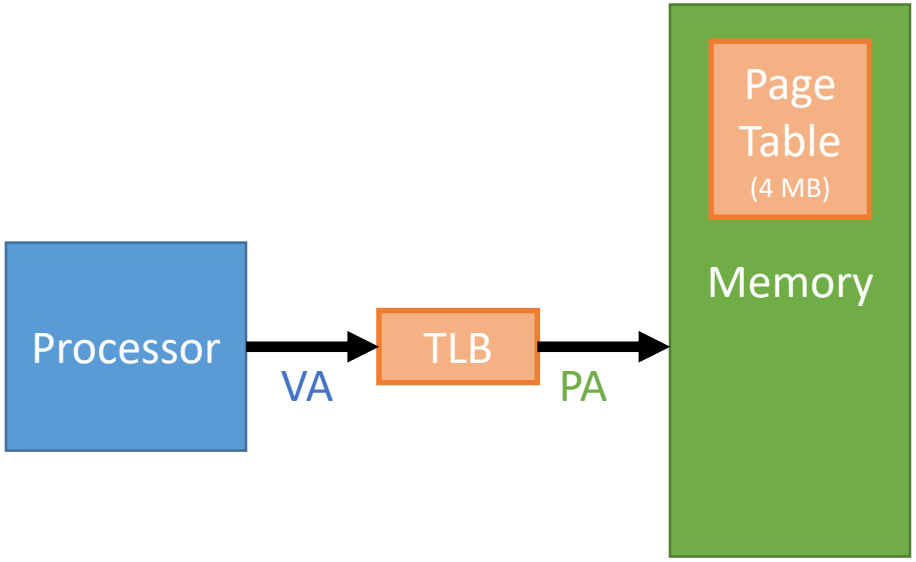

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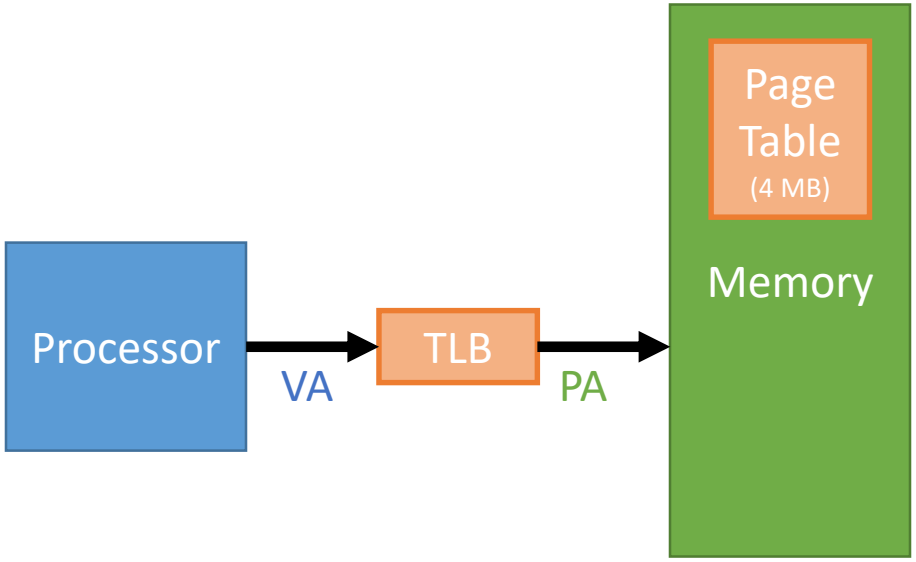

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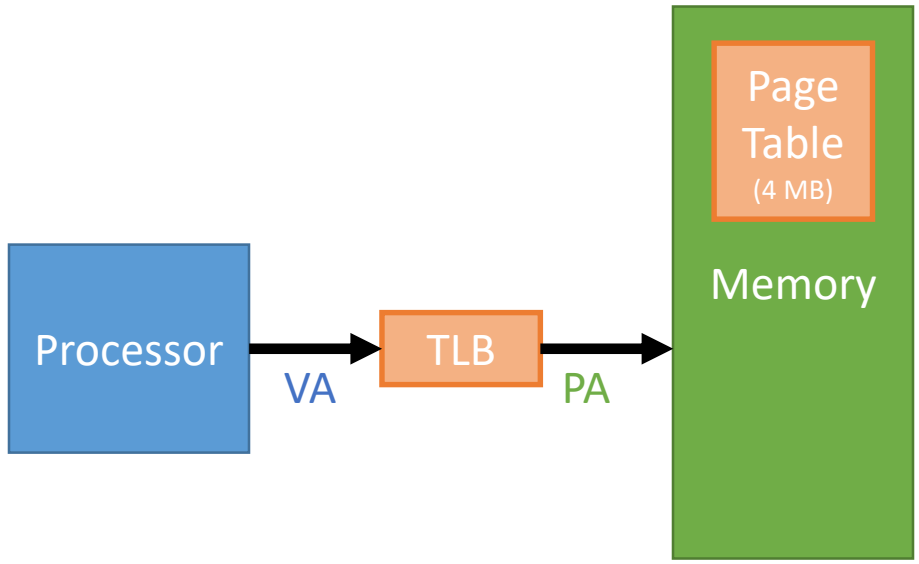

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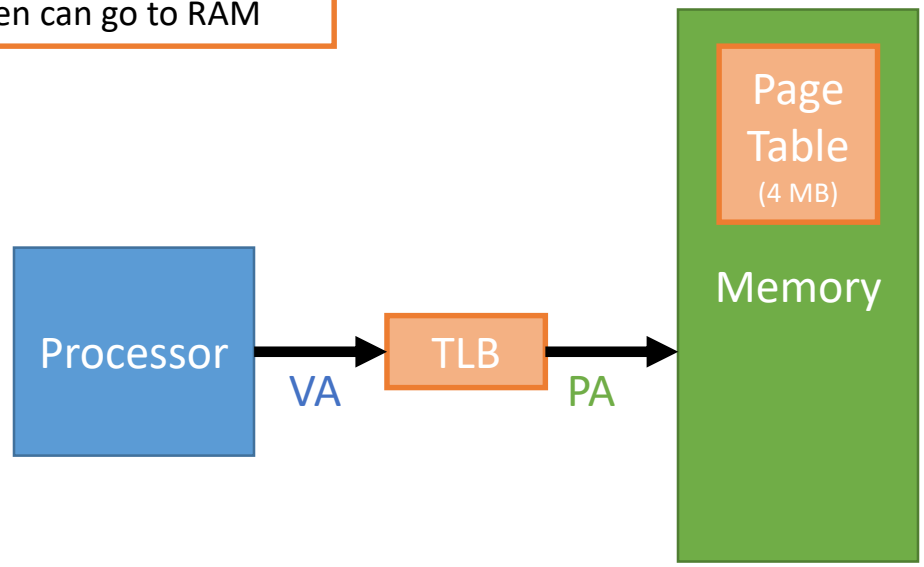

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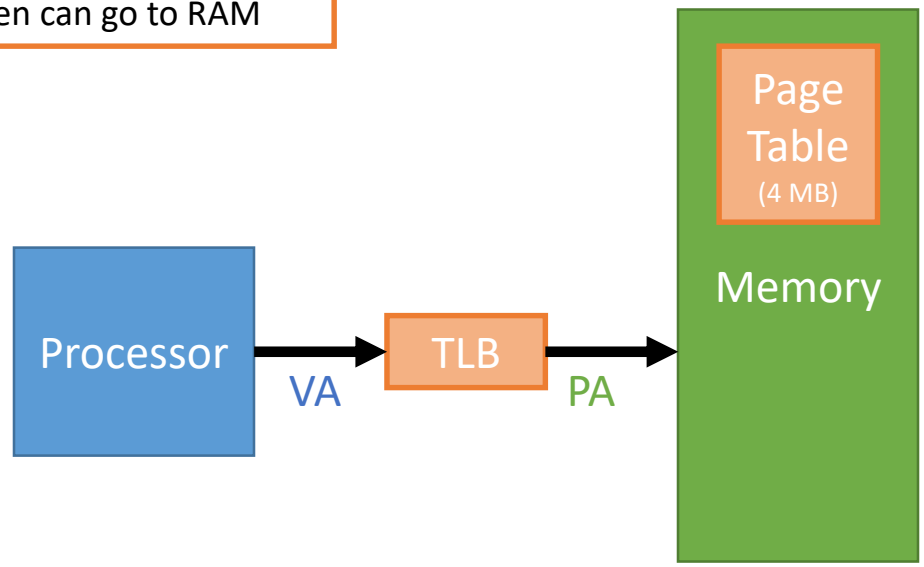

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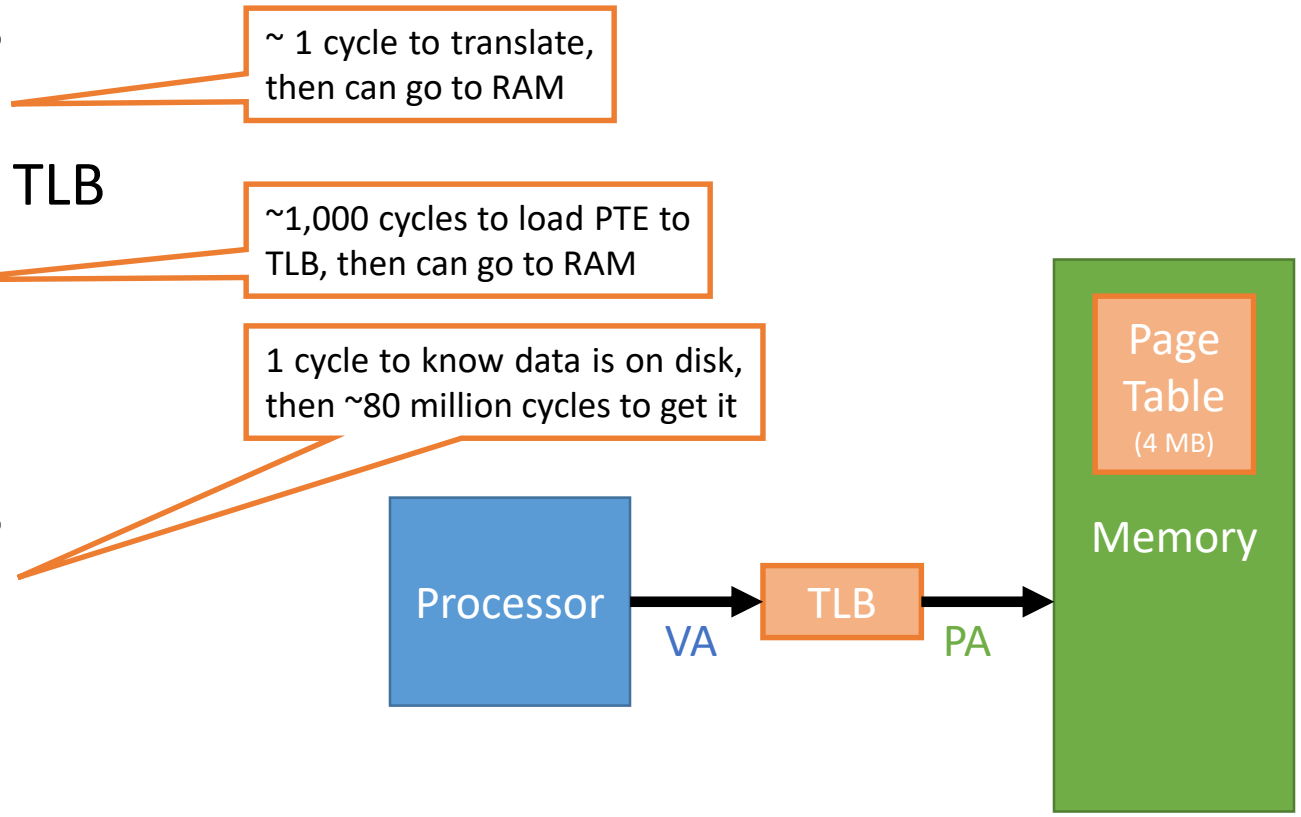

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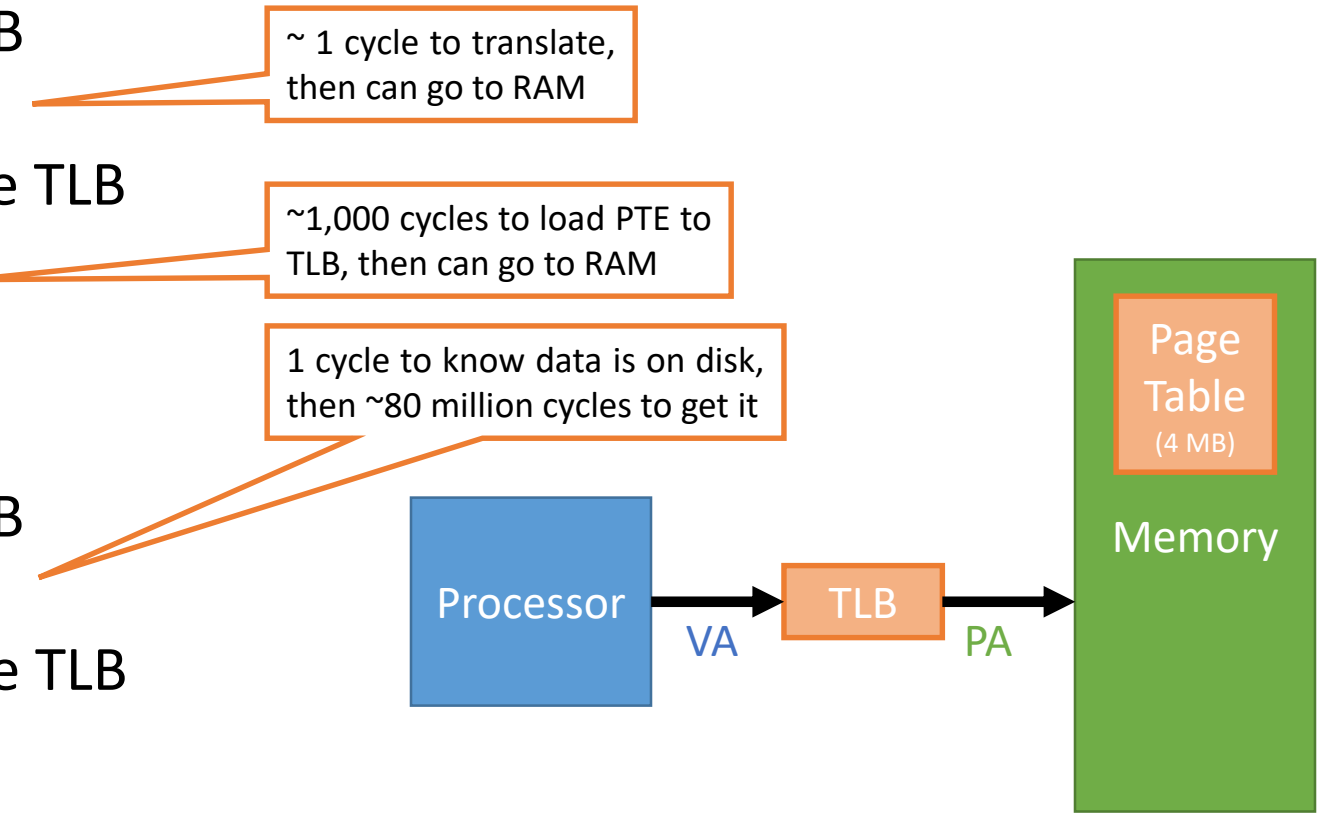

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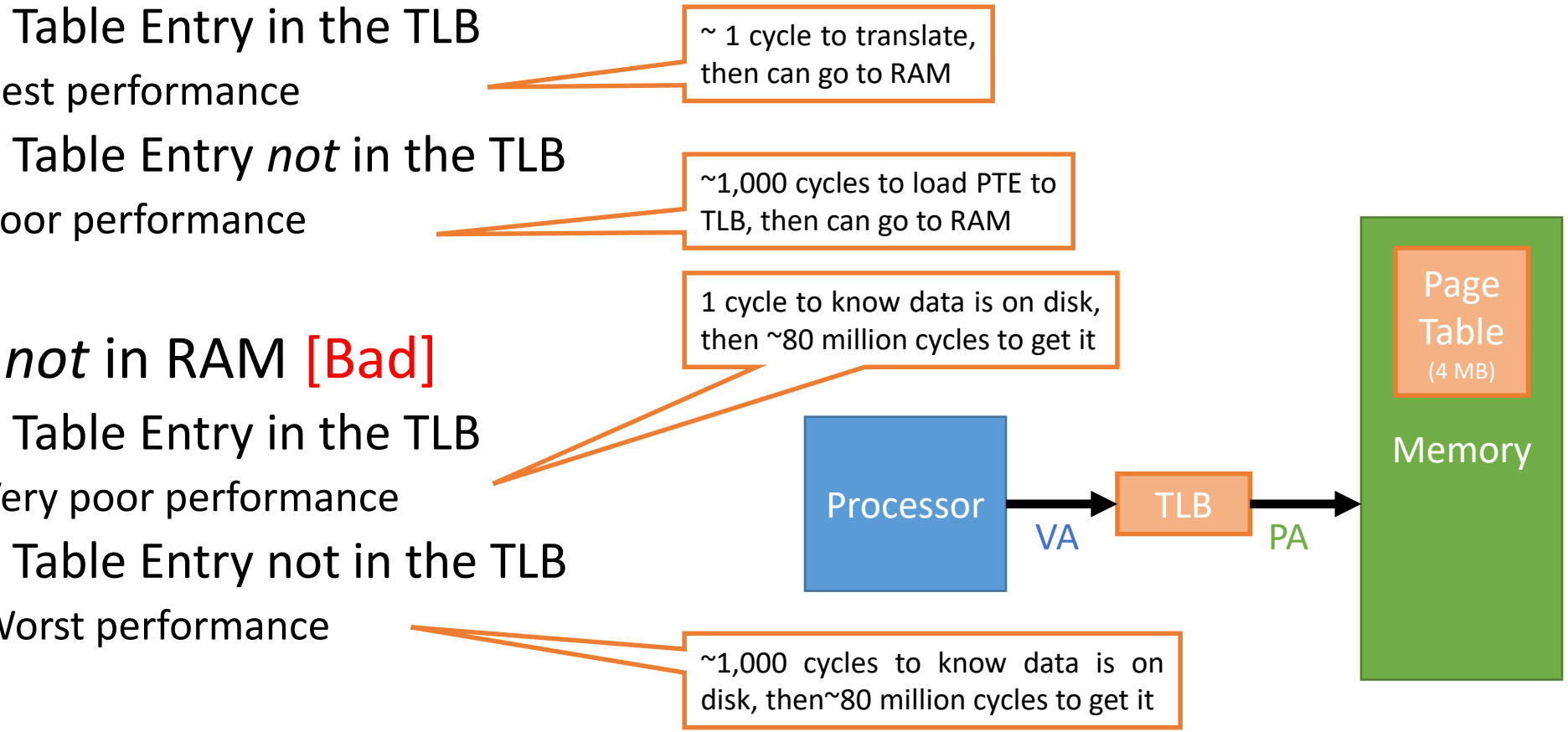

Illustration from the textbook

TLB	Page table	Cache	Possible? If so, under what circumstance?
Hit	Hit	Miss	Possible, although the page table is never really checked if TLB hits.
Miss	Hit	Hit	TLB misses, but entry found in page table; after retry, data is found in cache.
Miss	Hit	Miss	TLB misses, but entry found in page table; after retry, data misses in cache.
Miss	Miss	Miss	TLB misses and is followed by a page fault; after retry, data must miss in cache.
Hit	Miss	Miss	Impossible: cannot have a translation in TLB if page is not present in memory.
Hit	Miss	Hit	Impossible: cannot have a translation in TLB if page is not present in memory.
Miss	Miss	Hit	Impossible: data cannot be allowed in cache if the page is not in memory.

FIGURE 5.32 The possible combinations of events in the TLB, virtual memory system, and cache. Three of these combinations are impossible, and one is possible (TLB hit, virtual memory hit, cache miss) but never detected.

How do we make the TLB *seem* larger?

Q: How can we make the TLB appear larger without reducing performance?

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III. Add another TLB level
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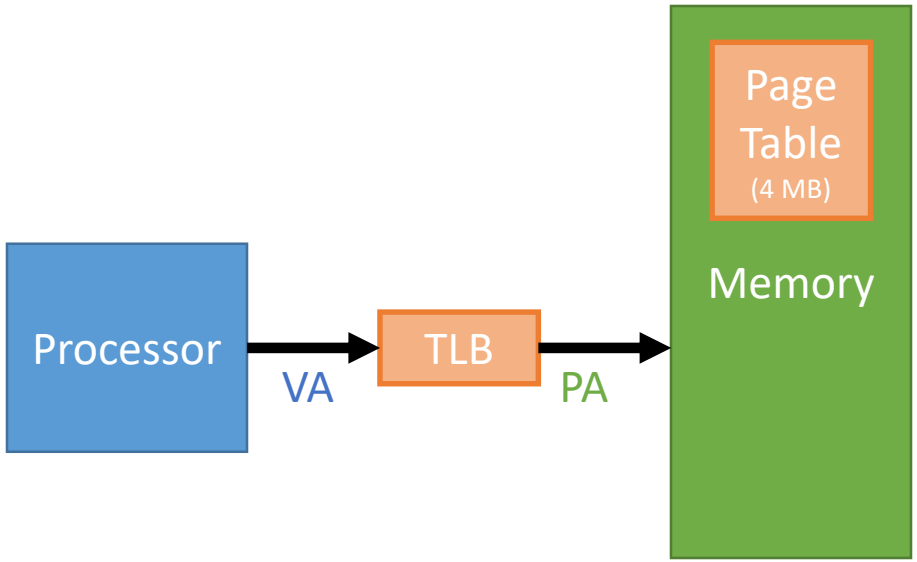

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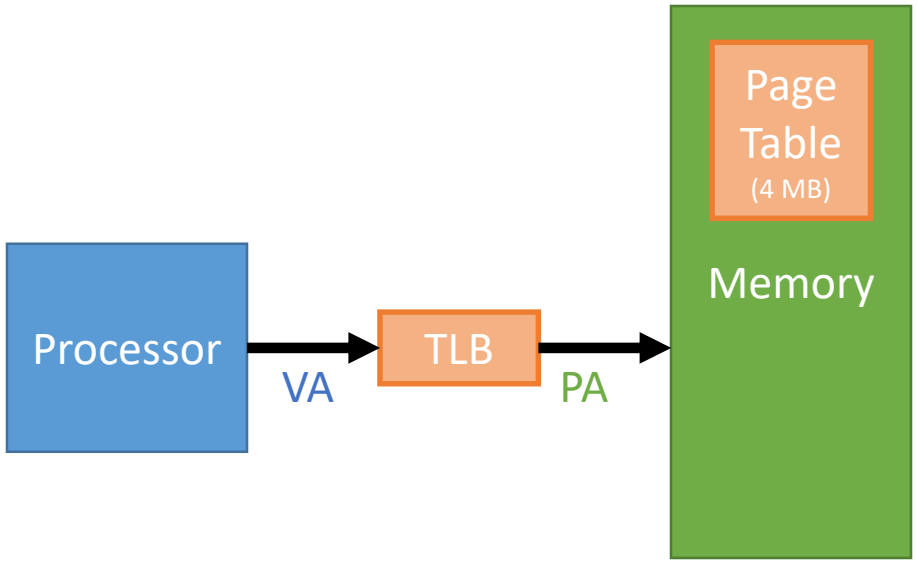

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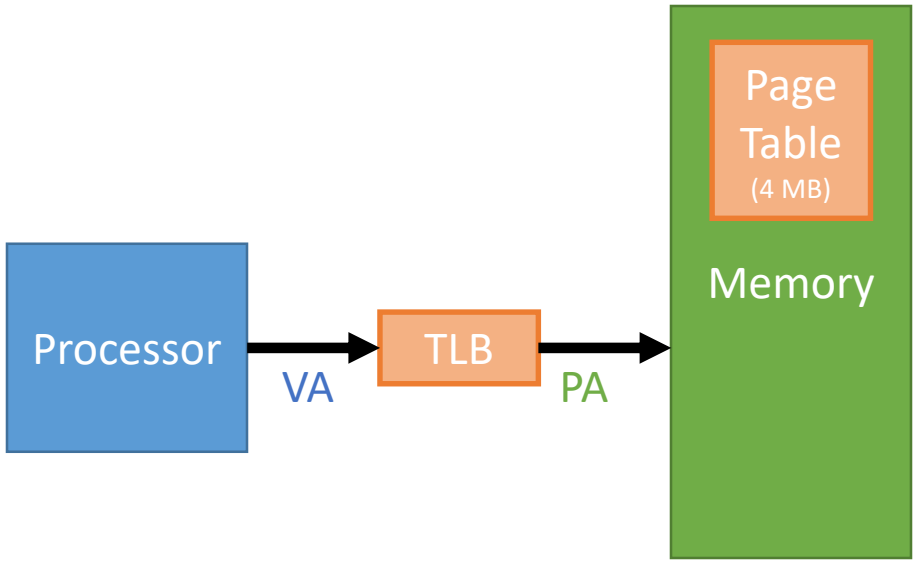

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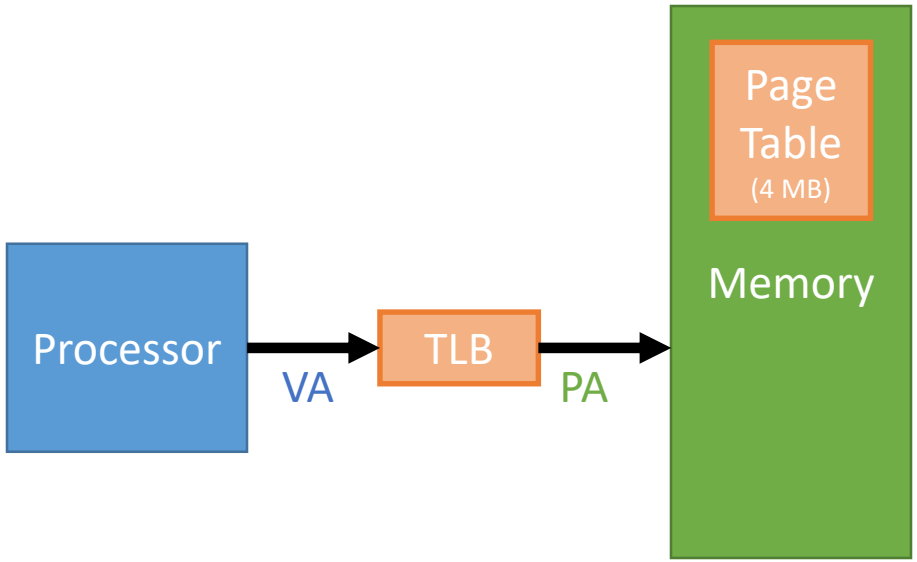

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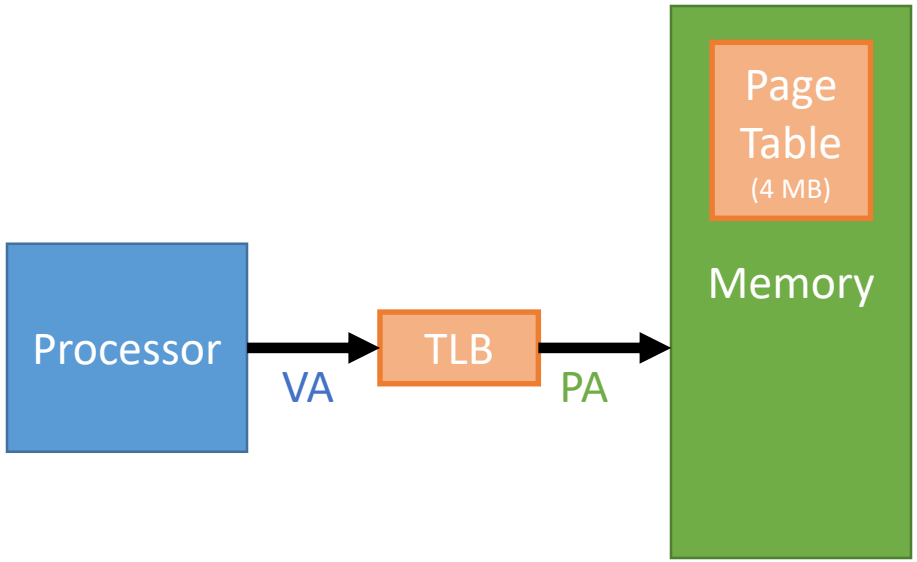

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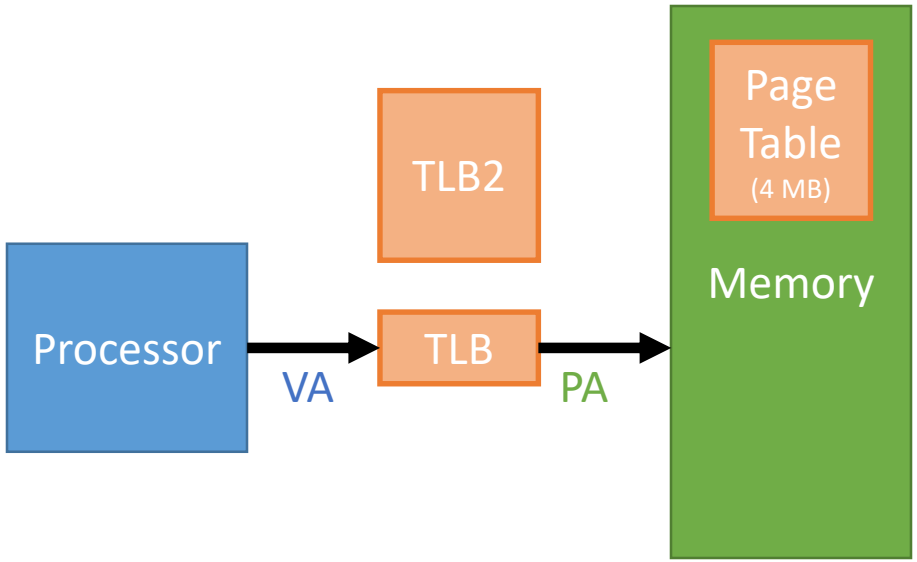

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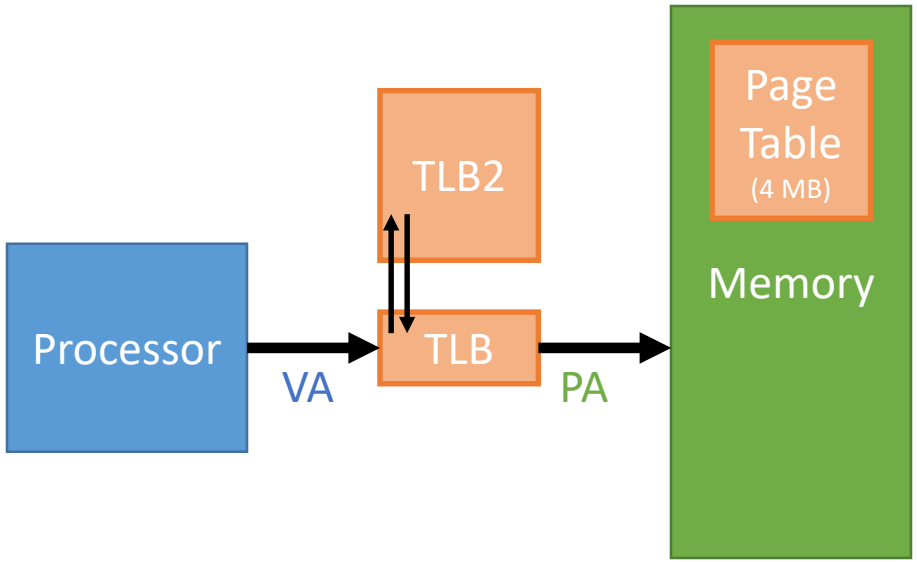

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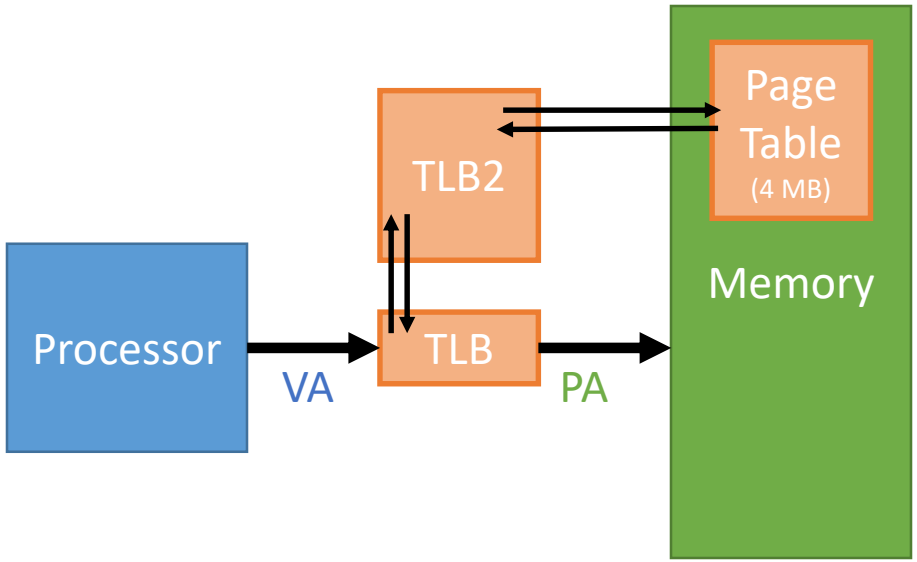

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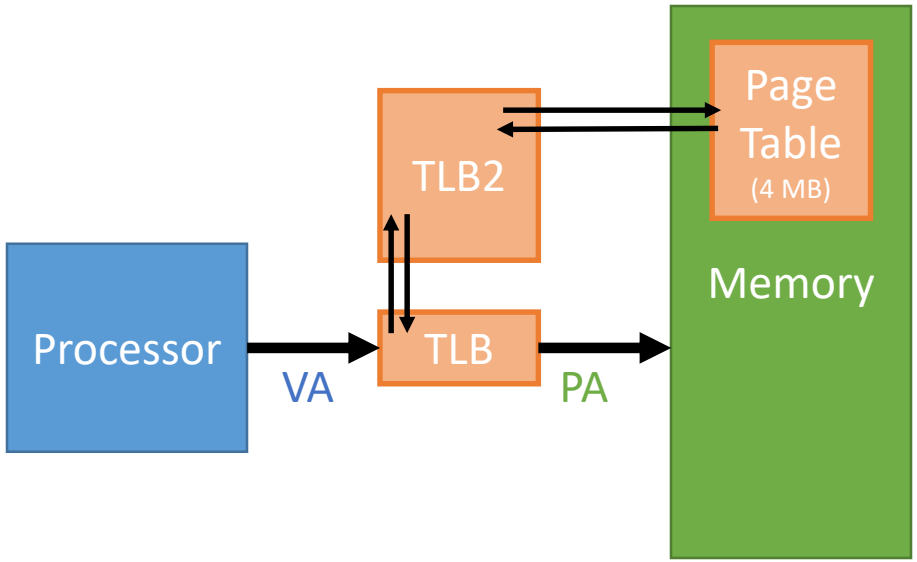

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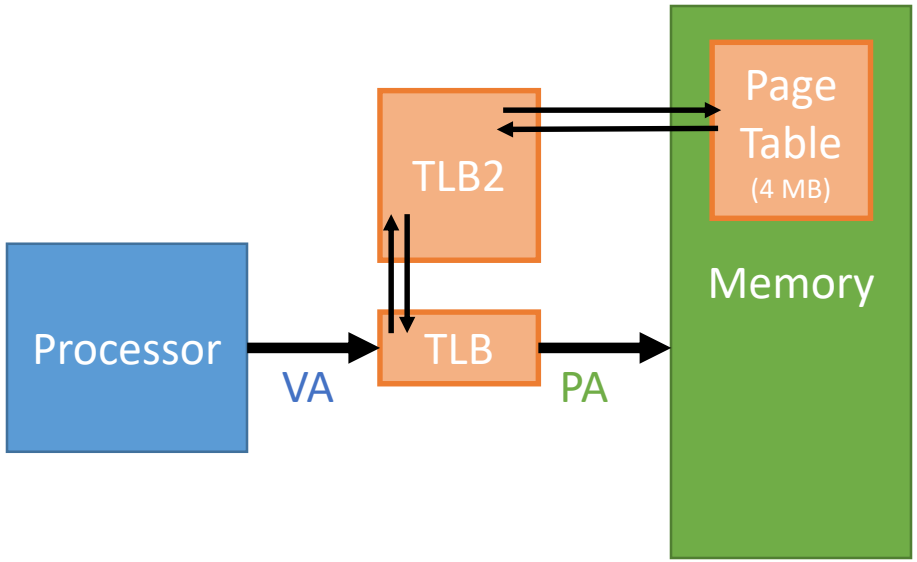

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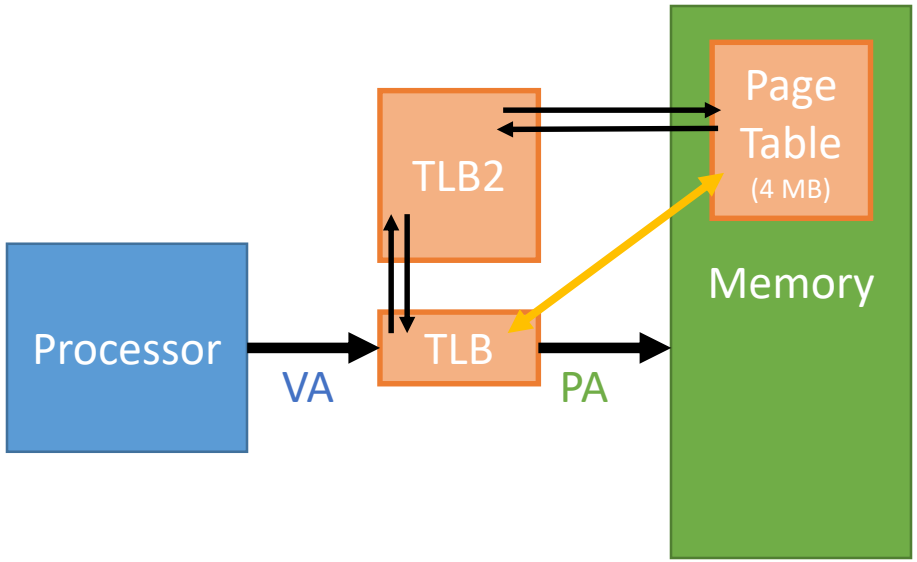

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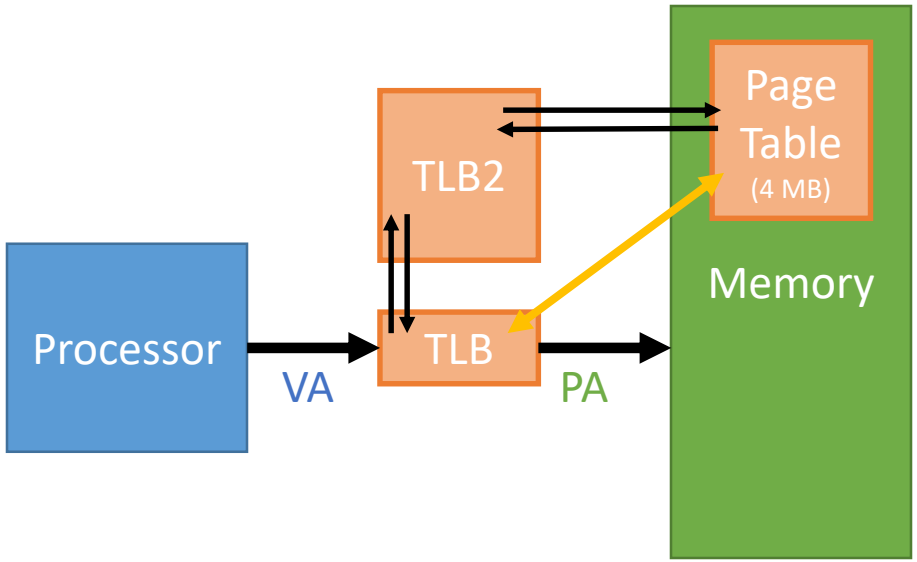

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Hardware can do a page table walk to replace a page in the TLB.

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